09/051263

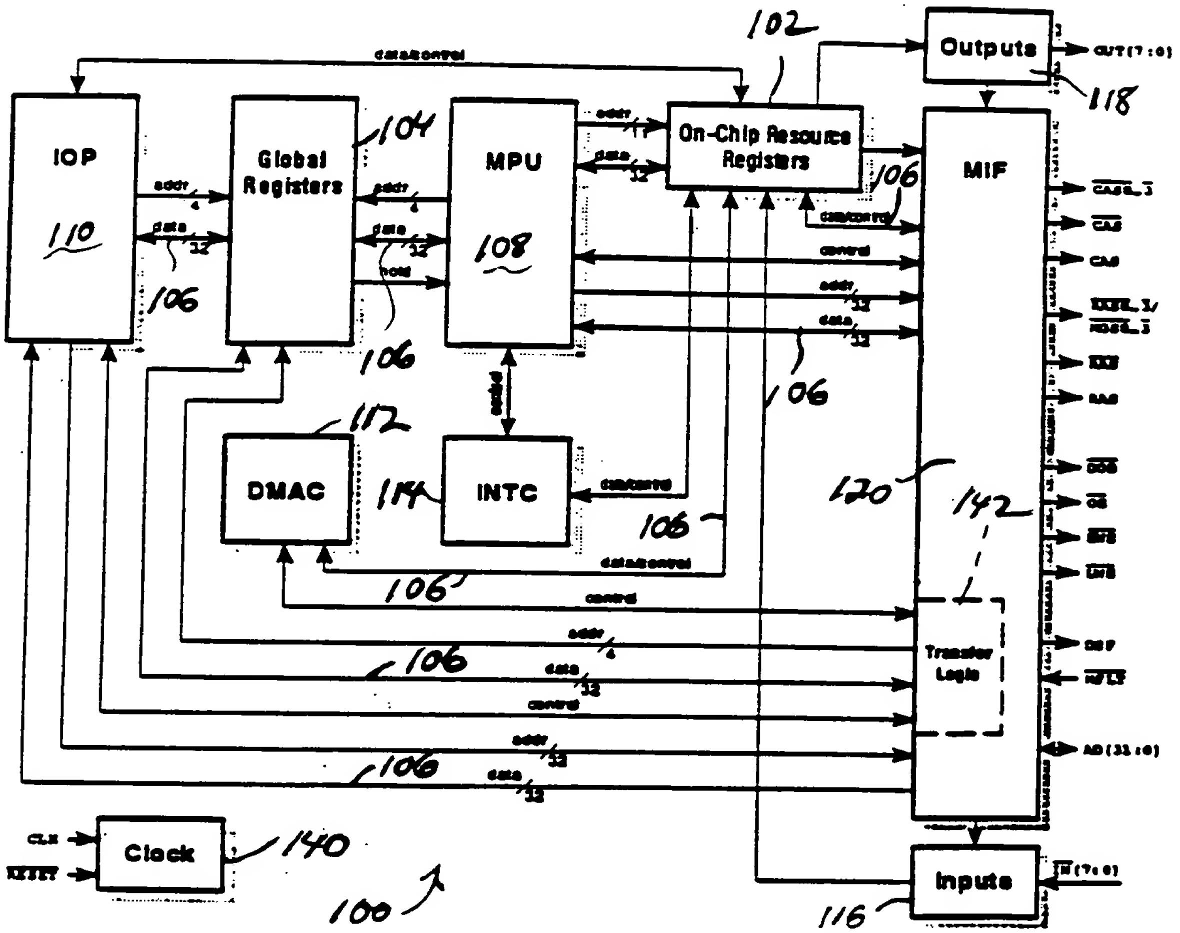

Fig. 1

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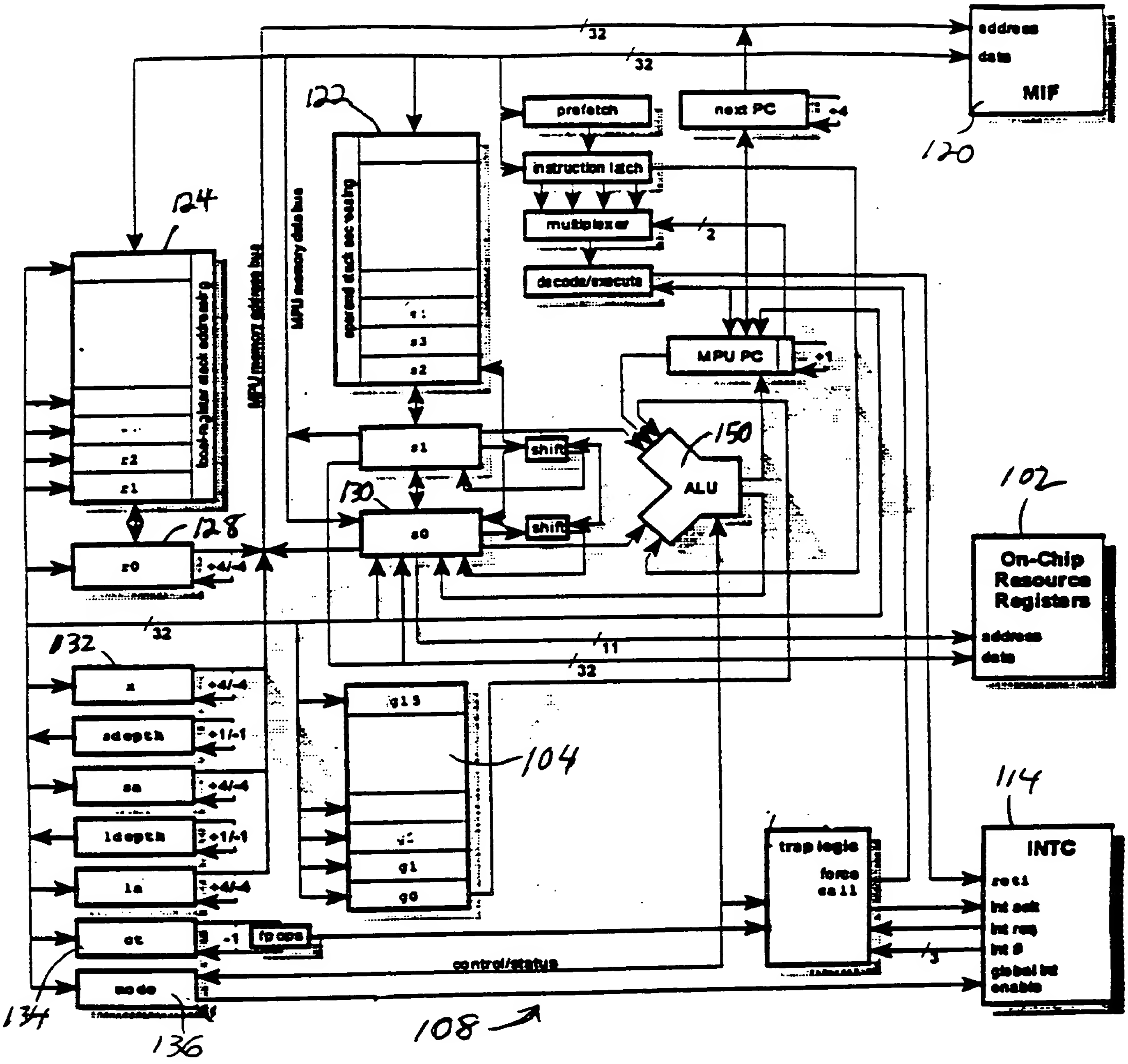

FIG. 2

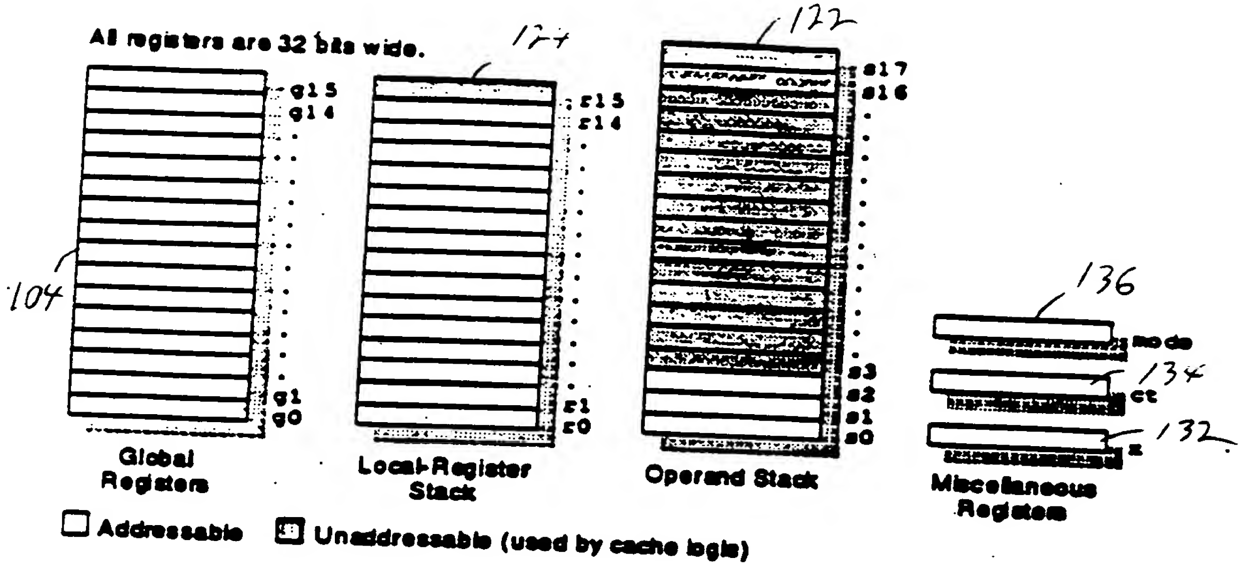
All registers are 32 bits wide.
124
122
g15
g14
g1
g0
r15
r14
r1
r0
s17
s16
s3
s2
s1
s0
104
136
mode
134
ct
132
x
Global Registers
Local-Register Stack
Operand Stack
Miscellaneous Registers
☐ Addressable
▨ Unaddressable (used by cache logic)

FIG. 3

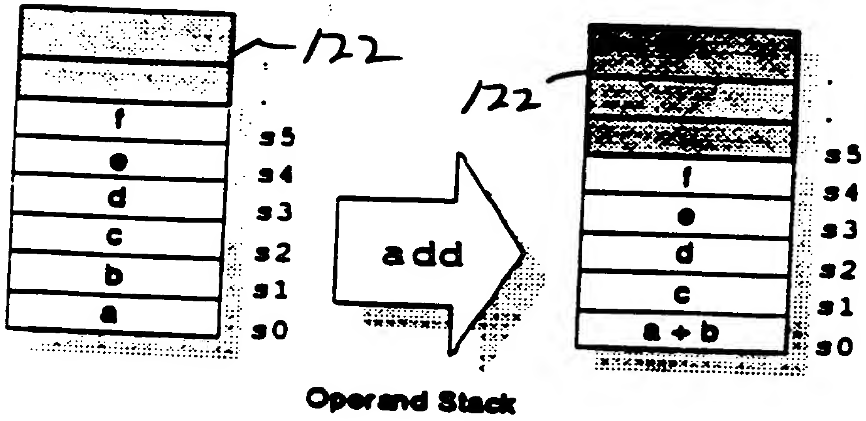
122
f
e
d
c
b
a
s5
s4
s3
s2
s1
s0
add
122
f
e
d
c
a + b
s5
s4
s3
s2
s1
s0
Operand Stack

FIG. 3a

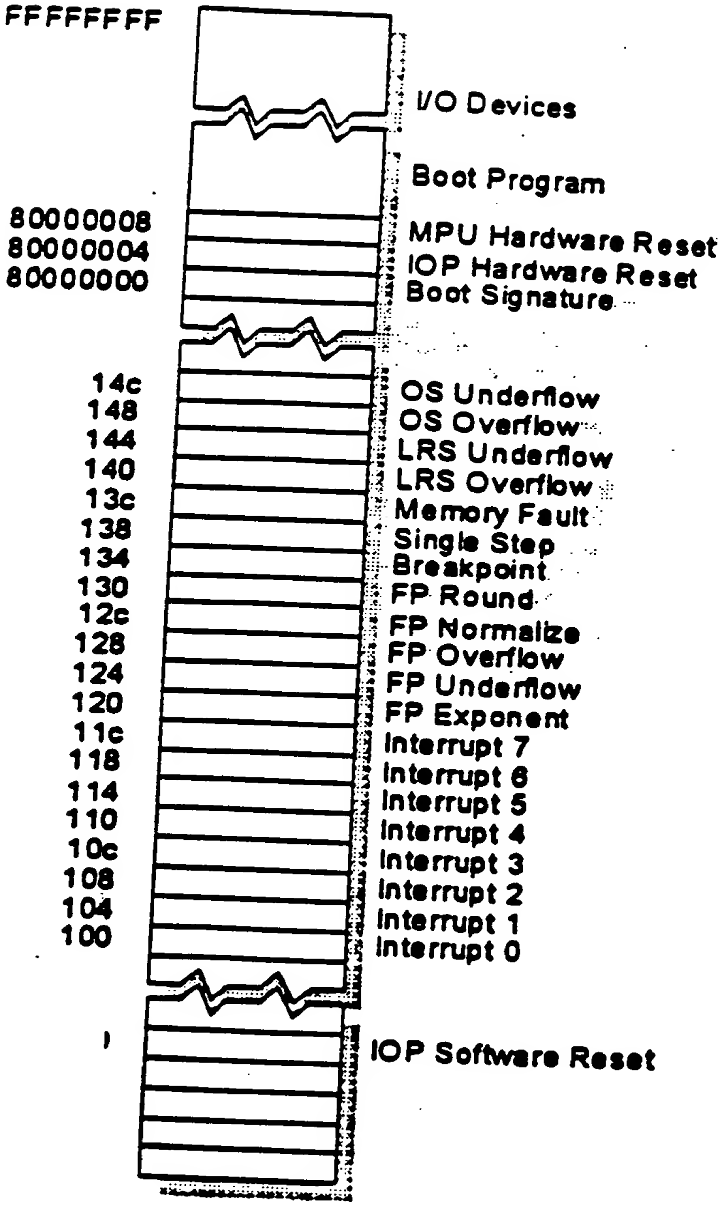
FFFFFFFF
I/O Devices
Boot Program
80000008
80000004
80000000
MPU Hardware Reset
IOP Hardware Reset
Boot Signature
14c
148
144
140
13c
138
134
130
12c
128
124
120
11c
118
114
110
10c
108
104
100
OS Underflow
OS Overflow
LRS Underflow
LRS Overflow
Memory Fault
Single Step
Breakpoint
FP Round
FP Normalize
FP Overflow
FP Underflow
FP Exponent
Interrupt 7
Interrupt 6
Interrupt 5
Interrupt 4
Interrupt 3
Interrupt 2
Interrupt 1
Interrupt 0
0
IOP Software Reset

FIG. 4

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5750

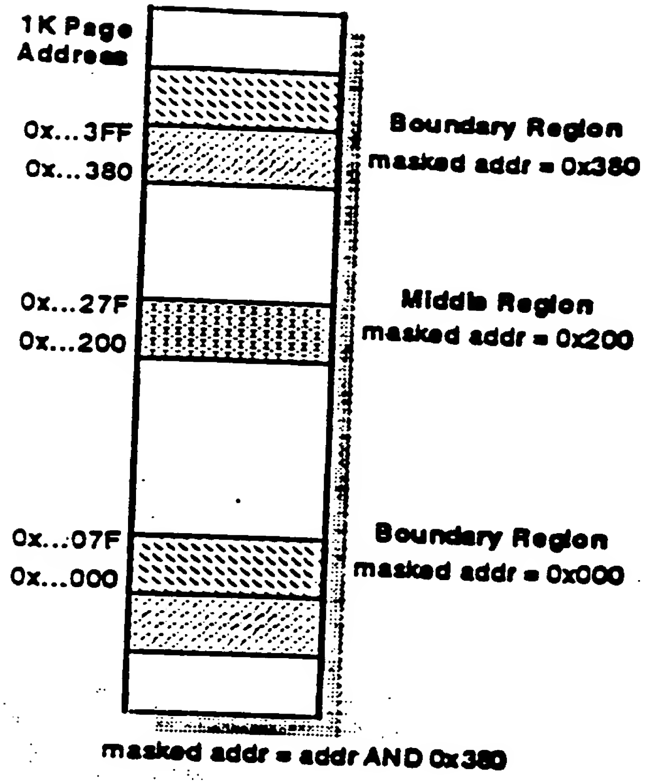


FIG. 5

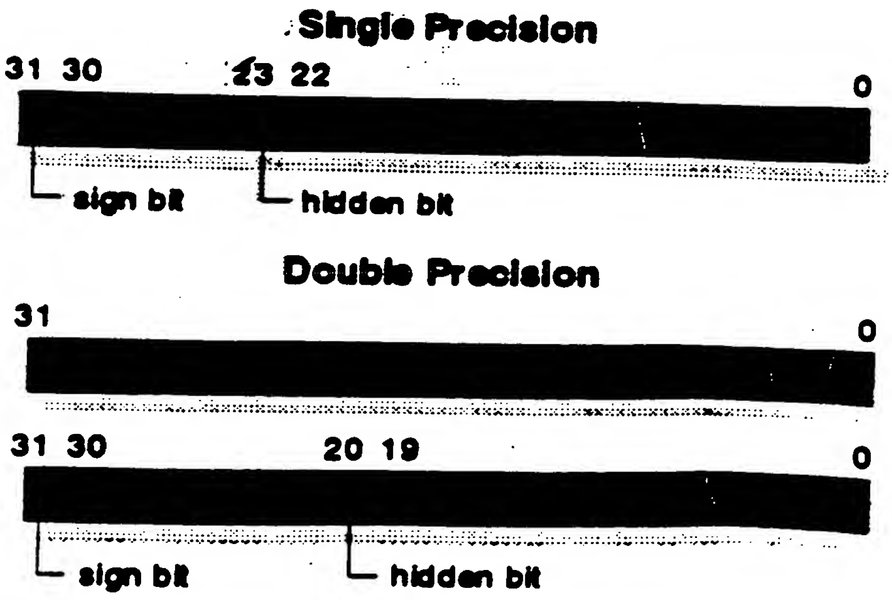


FIG. 6a

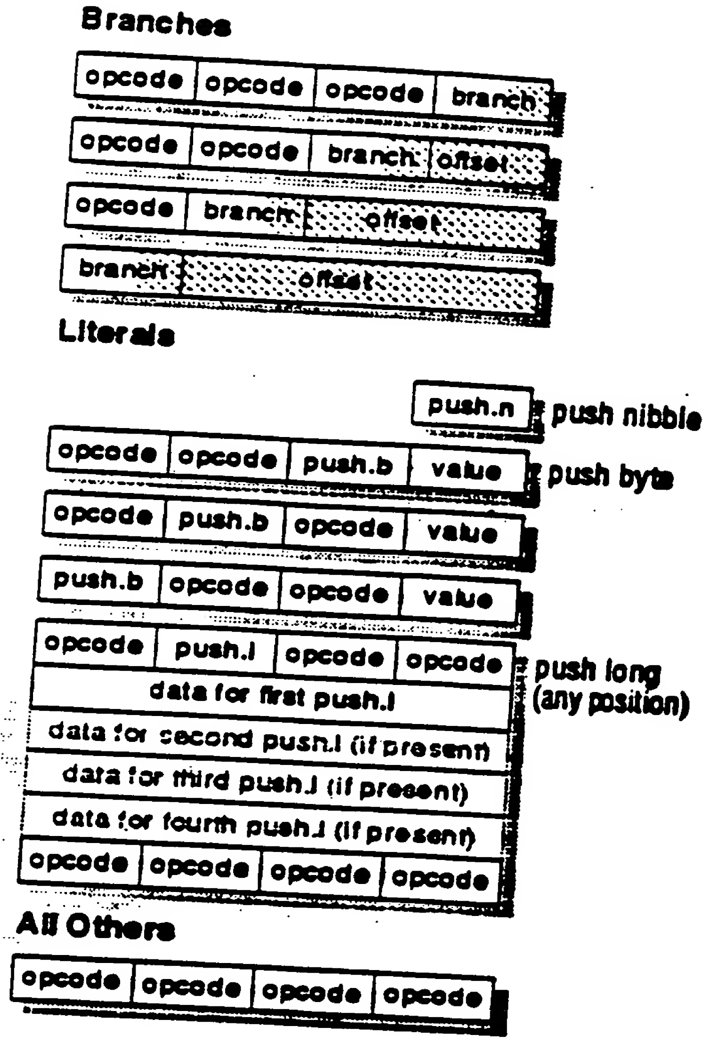
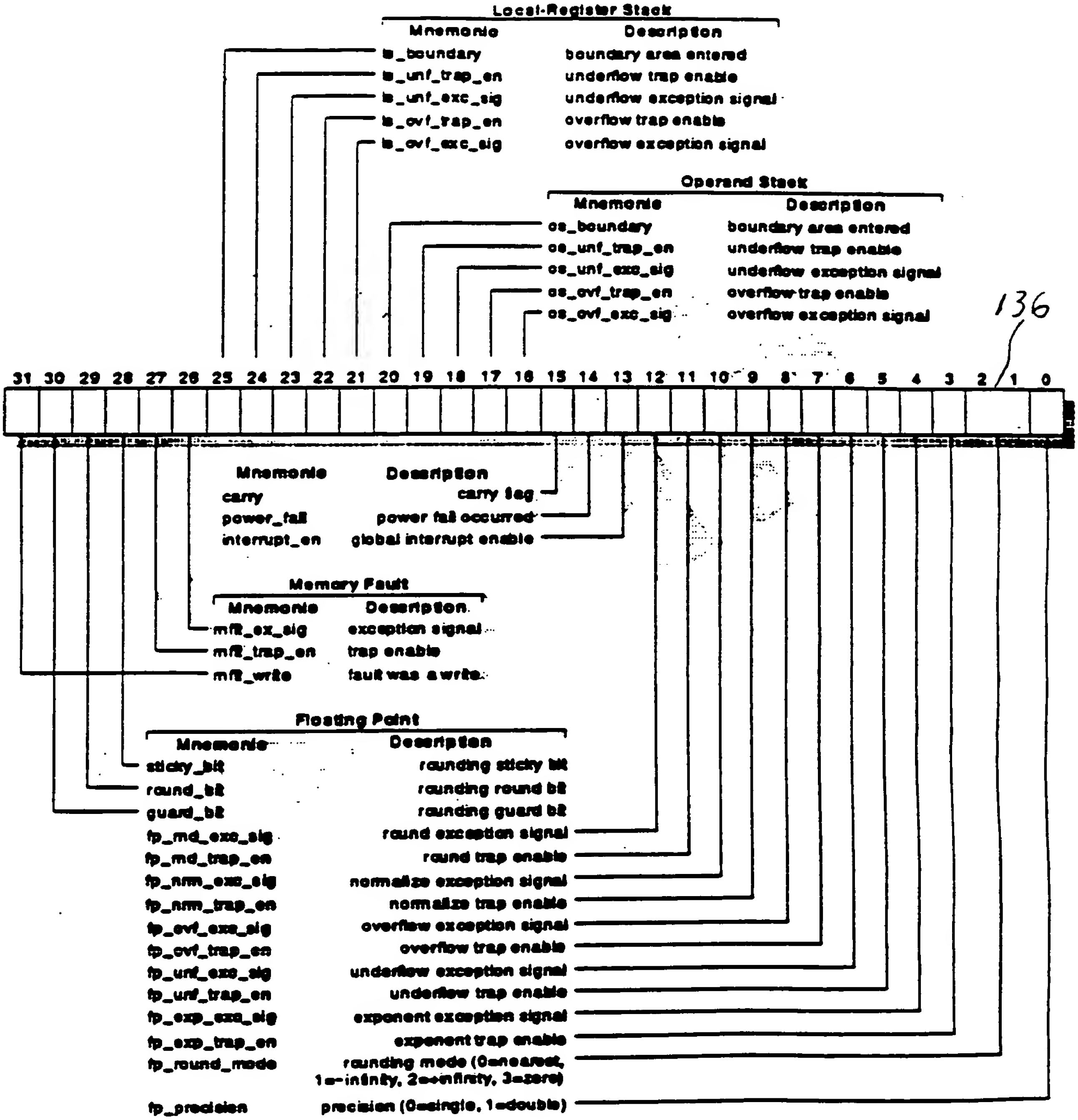

Branches
opcode
opcode
opcode
branch
opcode
opcode
branch
offset
opcode
branch
offset
branch
offset
Literals
push.n
push nibble
opcode
opcode
push.b
value
push byte
opcode
push.b
opcode
value
push.b
opcode
opcode
value
opcode
push.l
opcode
opcode
push long
(any position)
data for first push.l
data for second push.l (if present)
data for third push.l (if present)
data for fourth push.l (if present)
opcode
opcode
opcode
opcode
All Others
opcode
opcode
opcode
opcode

FIG. 6



Local-Register Stack

| Mnemonic | Description |
|---|---|
| ls_boundary | boundary area entered |
| ls_unf_trap_en | underflow trap enable |
| ls_unf_exc_sig | underflow exception signal |
| ls_ovf_trap_en | overflow trap enable |
| ls_ovf_exc_sig | overflow exception signal |

Operand Stack

| Mnemonic | Description |
|---|---|
| os_boundary | boundary area entered |
| os_unf_trap_en | underflow trap enable |
| os_unf_exc_sig | underflow exception signal |
| os_ovf_trap_en | overflow trap enable |
| os_ovf_exc_sig | overflow exception signal |

| Mnemonic | Description |
|---|---|
| carry | carry flag |
| power_fail | power fail occurred |
| interrupt_en | global interrupt enable |

Memory Fault

| Mnemonic | Description |
|---|---|
| mflt_ex_sig | exception signal |
| mflt_trap_en | trap enable |
| mflt_write | fault was a write |

Floating Point

| Mnemonic | Description |
|---|---|
| sticky_bit | rounding sticky bit |
| round_bit | rounding round bit |
| guard_bit | rounding guard bit |
| fp_rnd_exc_sig | round exception signal |
| fp_rnd_trap_en | round trap enable |
| fp_nrm_exc_sig | normalize exception signal |
| fp_nrm_trap_en | normalize trap enable |
| fp_ovf_exc_sig | overflow exception signal |
| fp_ovf_trap_en | overflow trap enable |
| fp_unf_exc_sig | underflow exception signal |
| fp_unf_trap_en | underflow trap enable |
| fp_exp_exc_sig | exponent exception signal |
| fp_exp_trap_en | exponent trap enable |
| fp_round_mode | rounding mode (0=nearest, 1=-infinity, 2=+infinity, 3=zero) |
| fp_precision | precision (0=single, 1=double) |

FIG. 7

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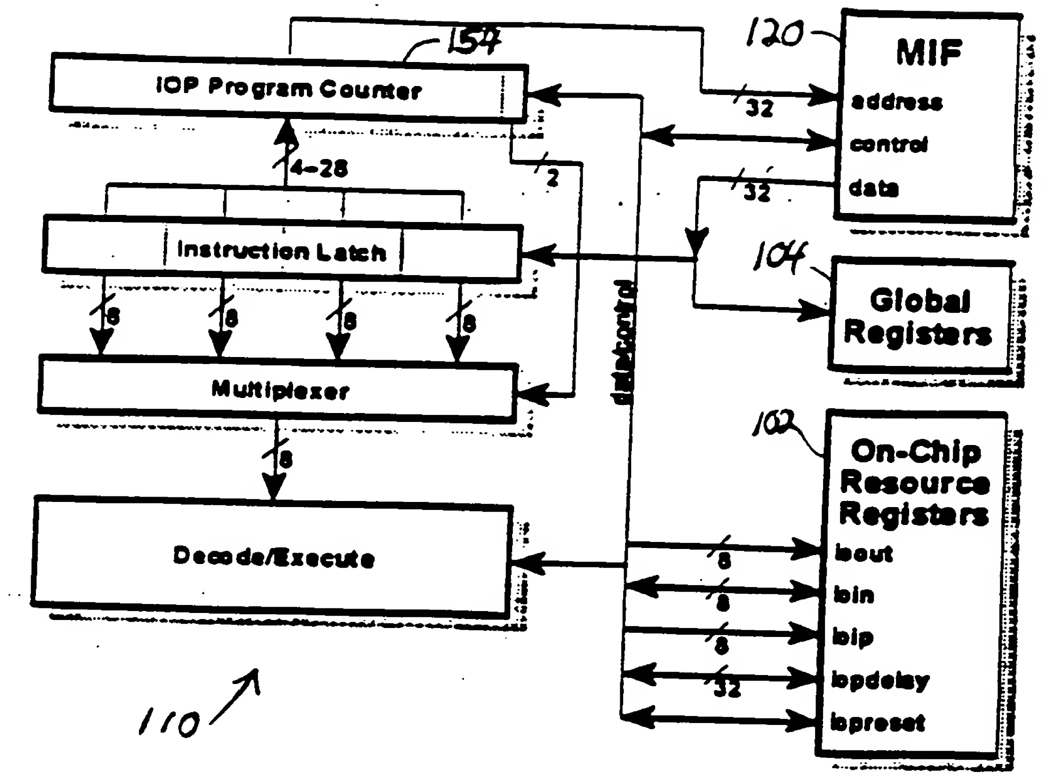

FIG. 8

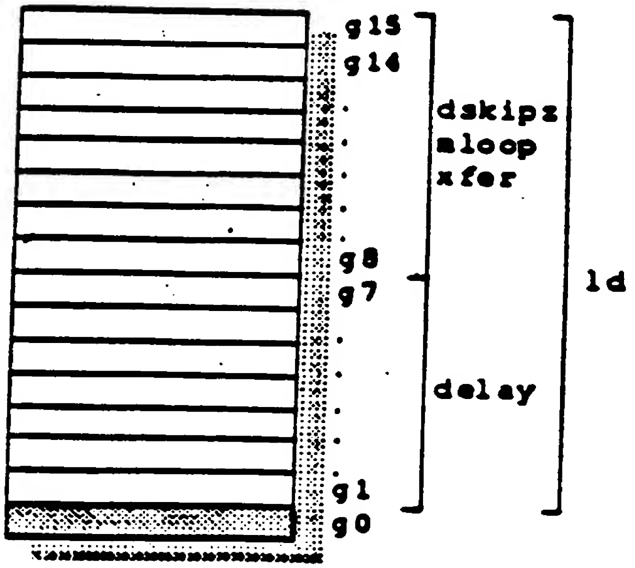

FIG. 9

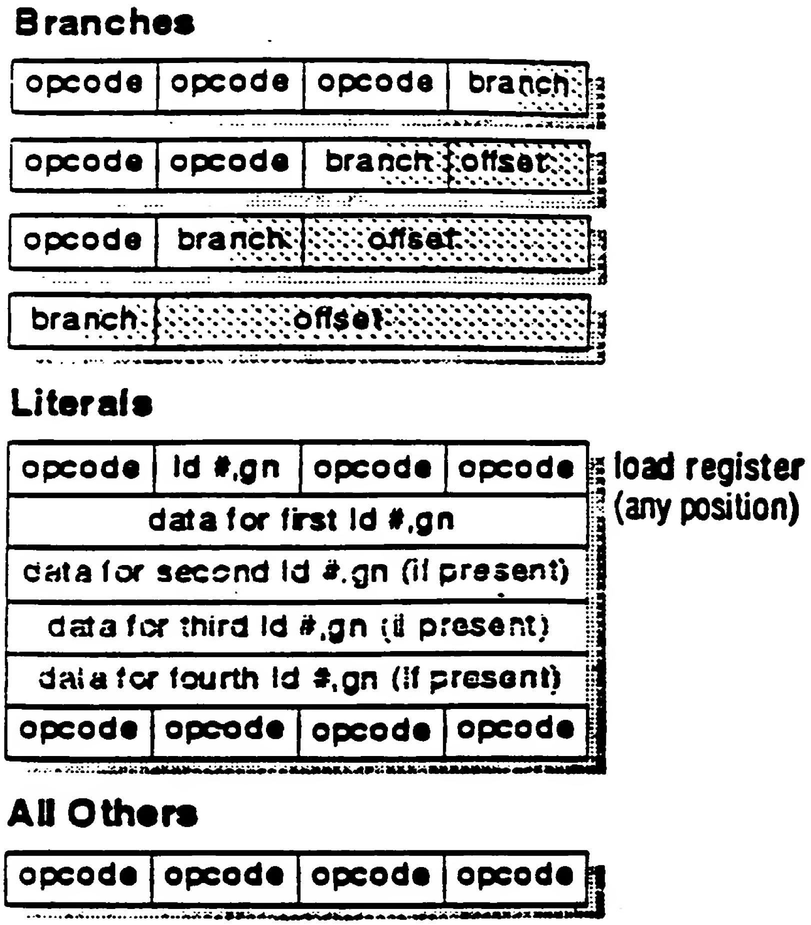
Branches
opcode
opcode
opcode
branch
opcode
opcode
branch
offset
opcode
branch
offset
branch
offset
Literals
opcode
ld #,gn
opcode
opcode
load register (any position)
data for first ld #,gn
data for second ld #,gn (if present)
data for third ld #,gn (if present)
data for fourth ld #,gn (if present)
opcode
opcode
opcode
opcode
All Others
opcode
opcode
opcode
opcode

FIG. 10

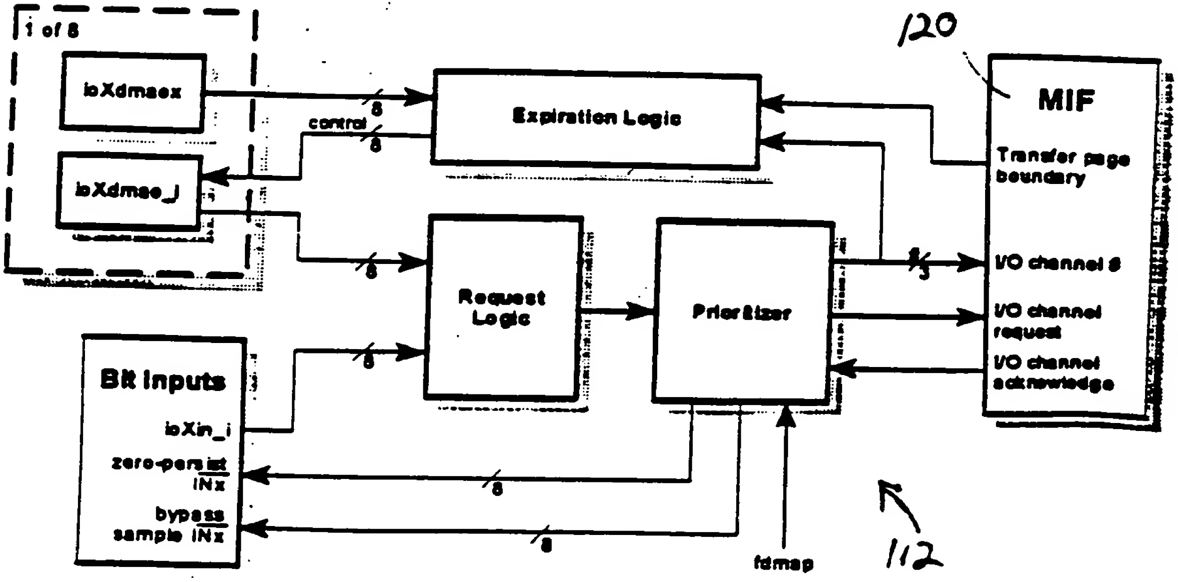
1 of 8
ioXdmaex
ioXdmae_i
control
8
8
8
8
Expiration Logic
Request Logic
Prioritizer
Bit Inputs
ioXin_i
zero-persist INx
bypass sample INx
8
8
fdmap
120
MIF
Transfer page boundary
I/O channel #
3
I/O channel request
I/O channel acknowledge
112

FIG. 11

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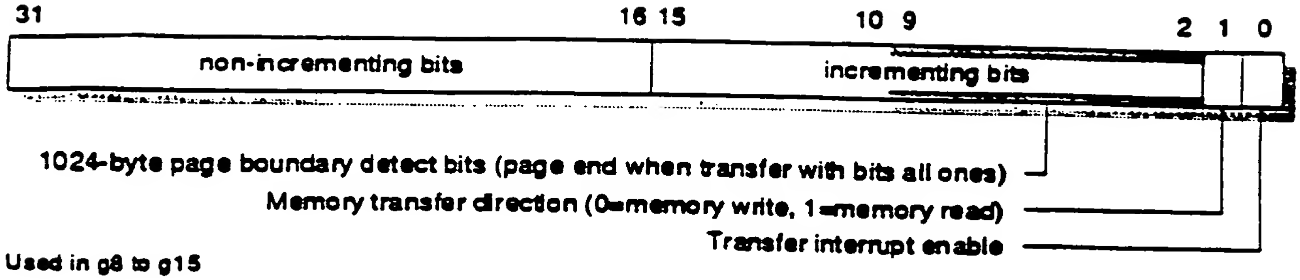

FIG. 12

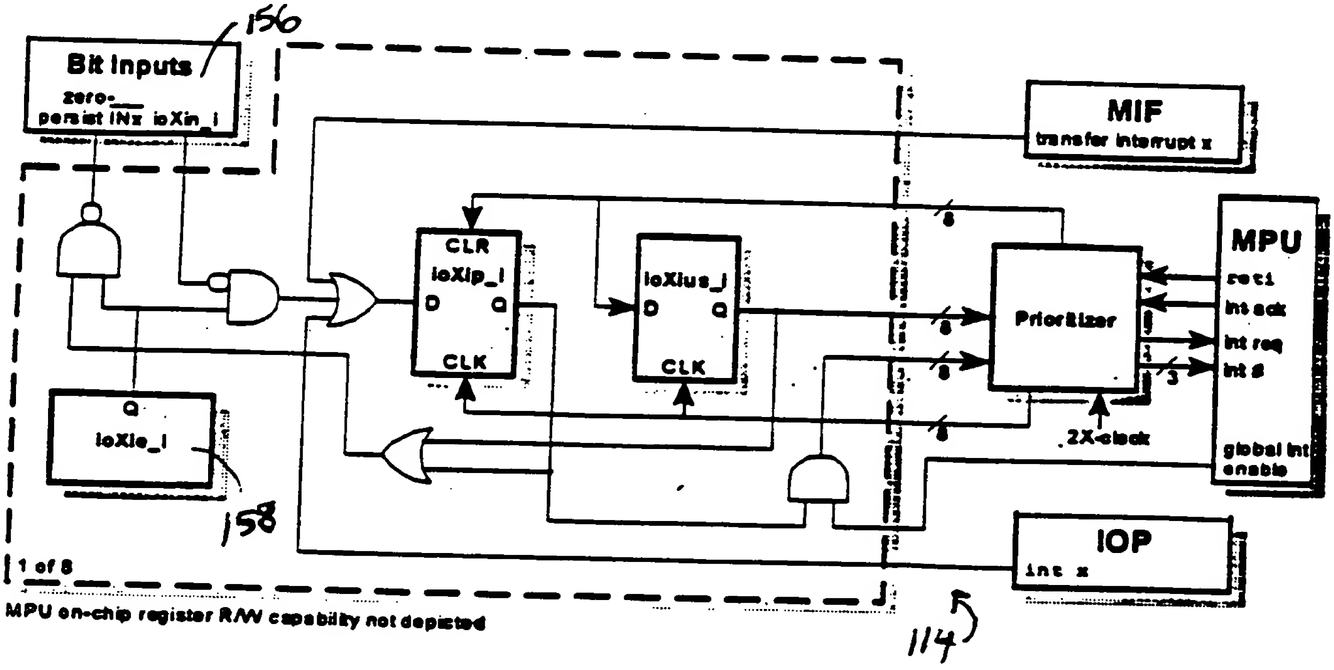

FIG. 13

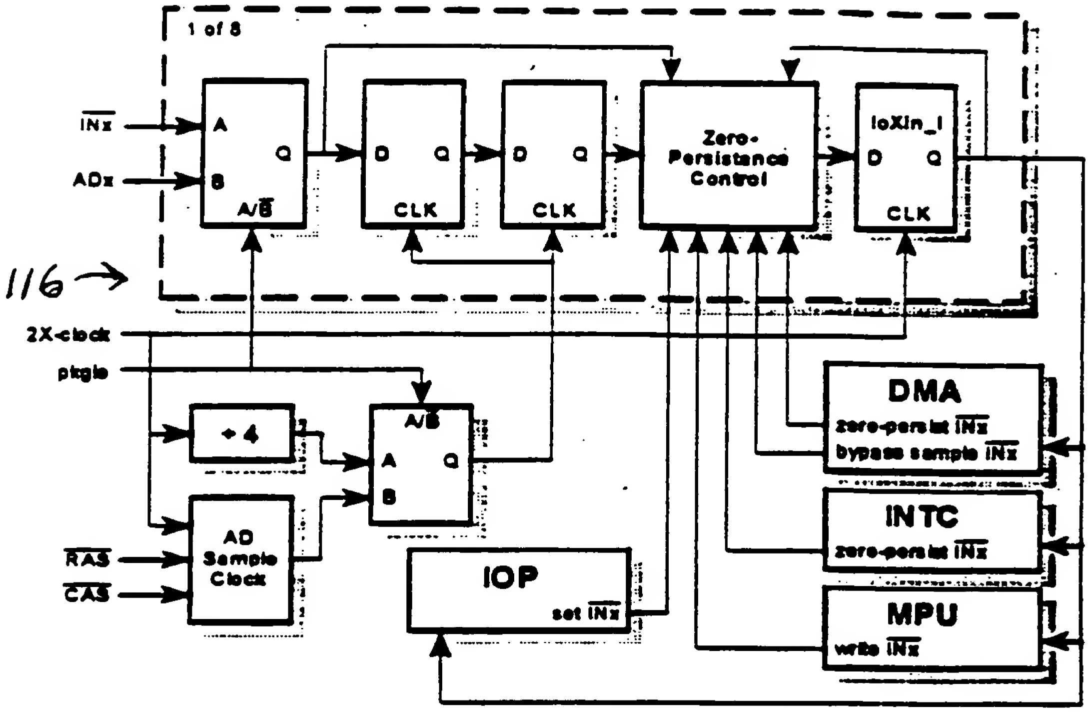
1 of 8
116
INx
ADx
A
B
Q
A/B
D
Q
CLK
D
Q
CLK
Zero-Persistence Control
IoXIn_I
D
Q
CLK
2X-clock
ptgle
÷4
A/B
A
B
Q
AD Sample Clock
RAS
CAS
IOP
set INx
DMA
zero-persist INx
bypass sample INx
INTC
zero-persist INx
MPU
write INx

FIG. 14

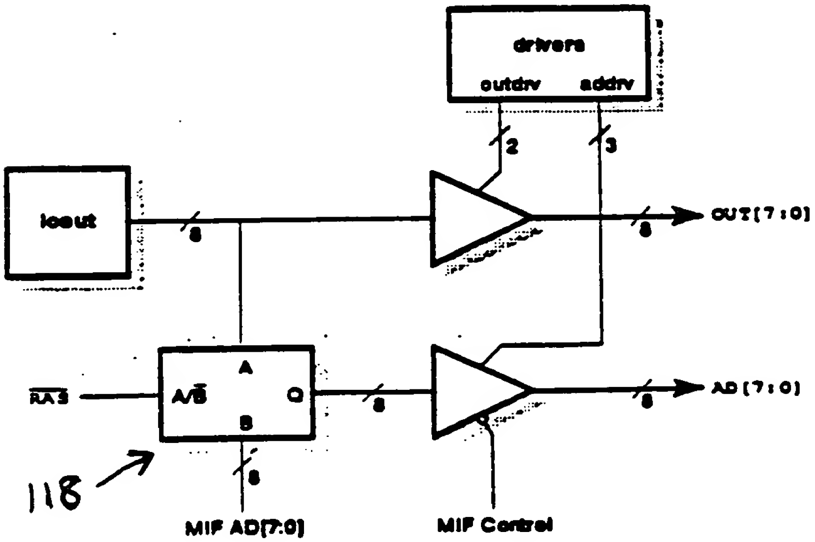
drivers
outdrv
addrv
2
3
ioout
8
OUT[7:0]
8
RAS
A/B
A
B
Q
8
8
AD[7:0]
8
118
MIF AD[7:0]
MIF Control

FIG. 15

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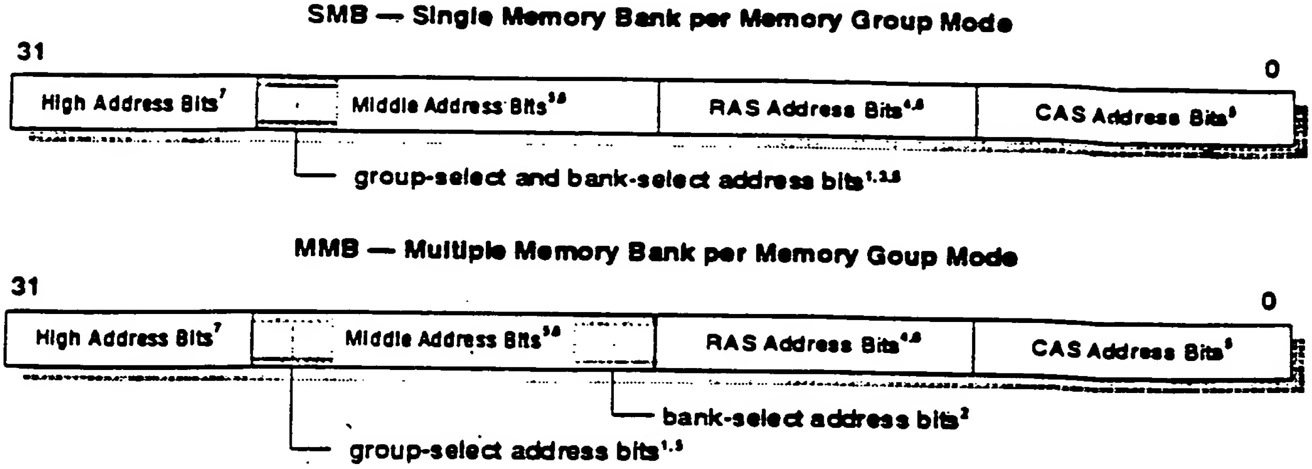

**Notes**

1. Located by bits in `msgsm`.
2. DRAM—2 bits immediately above the RAS address bits.
   SRAM—2 bits located by `mssbs` in `miscc`.
3. SRAM and DRAM.
4. DRAM only, field is zero length in SRAM .
5. Excluded from RAS-cycle determination, except for A31 (see note 7).
6. Included in RAS-cycle determination.
7. Optionally included in RAS-cycle determination.
8. If `msgsm` is zero, see text.

FIG. 16

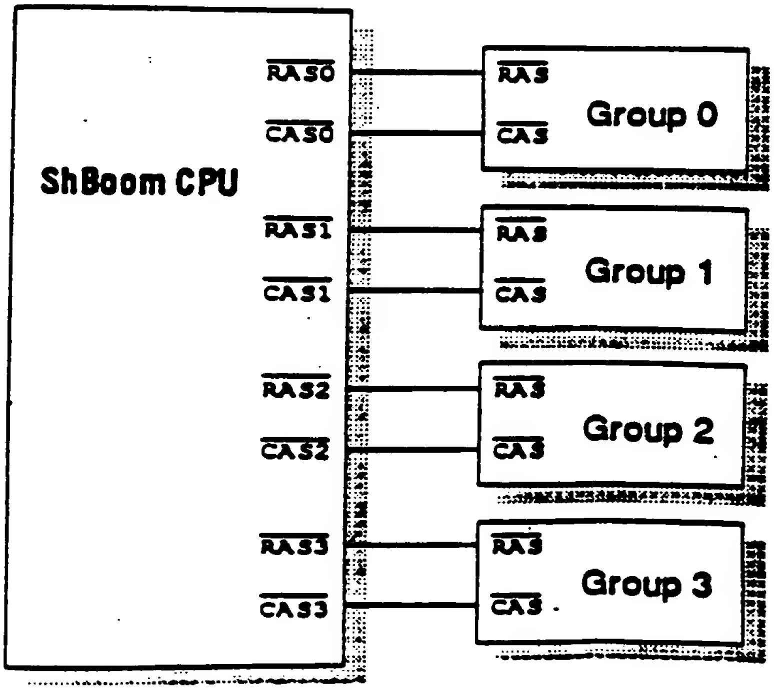

FIG. 17

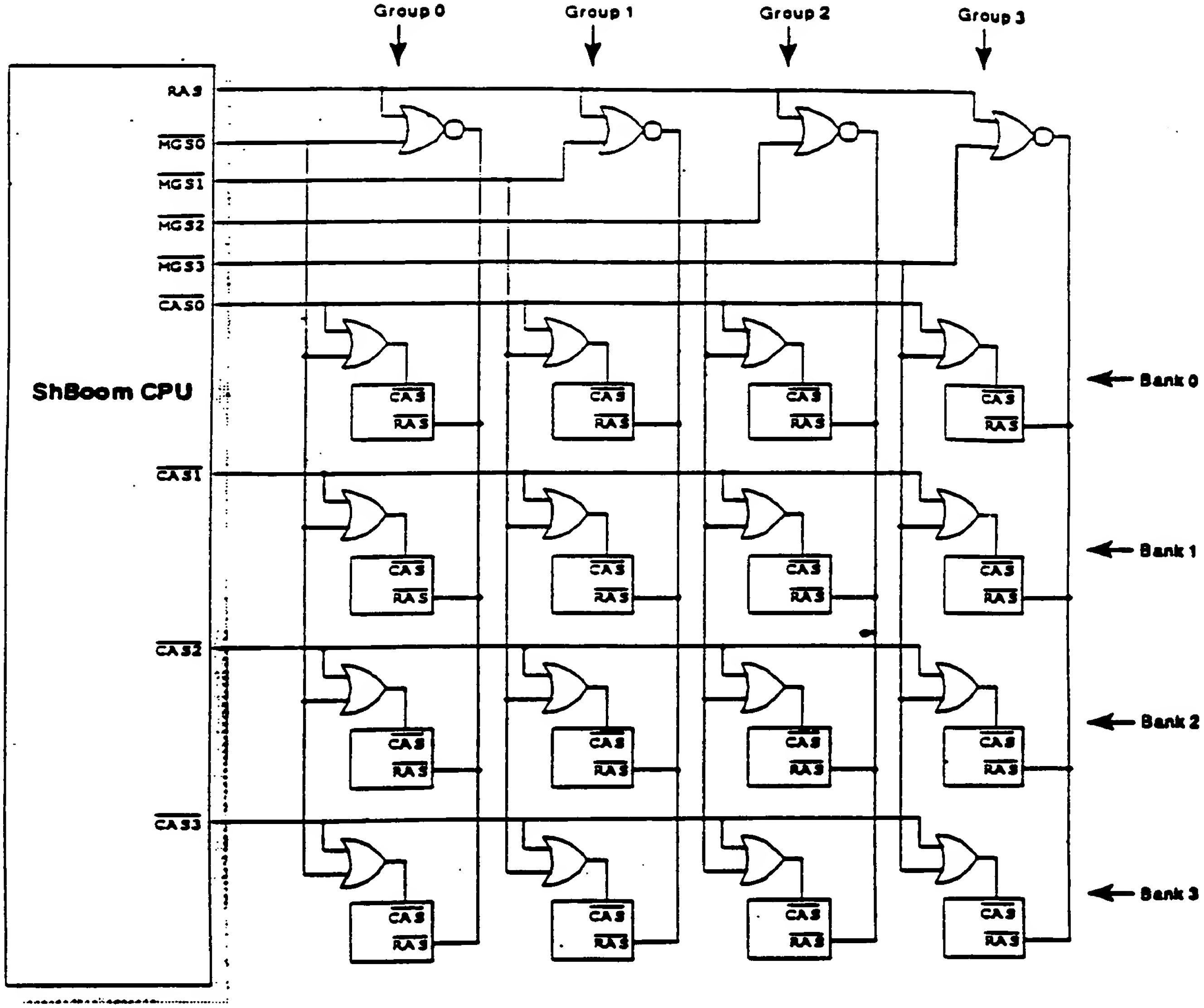
Group 0
Group 1
Group 2
Group 3
ShBoom CPU
RAS
$\overline{MGS0}$
$\overline{MGS1}$
$\overline{MGS2}$
$\overline{MGS3}$
$\overline{CAS0}$
$\overline{CAS1}$
$\overline{CAS2}$
$\overline{CAS3}$
$\overline{CAS}$
$\overline{RAS}$
Bank 0
Bank 1
Bank 2
Bank 3

FIG. 18

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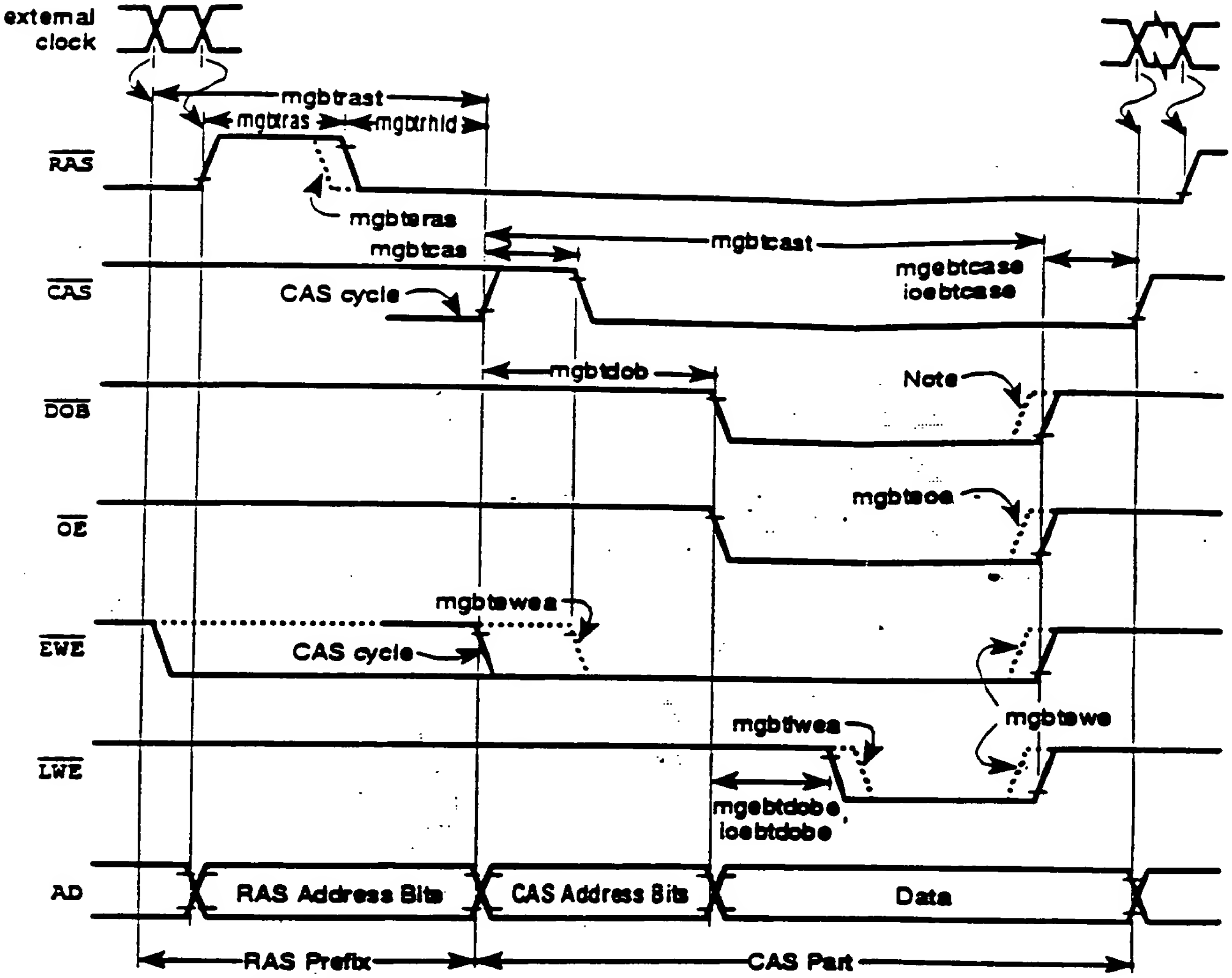

Note: –DOB rise tracks –OE and –EARLYWE/–LATEWE rise.

FIG. 19

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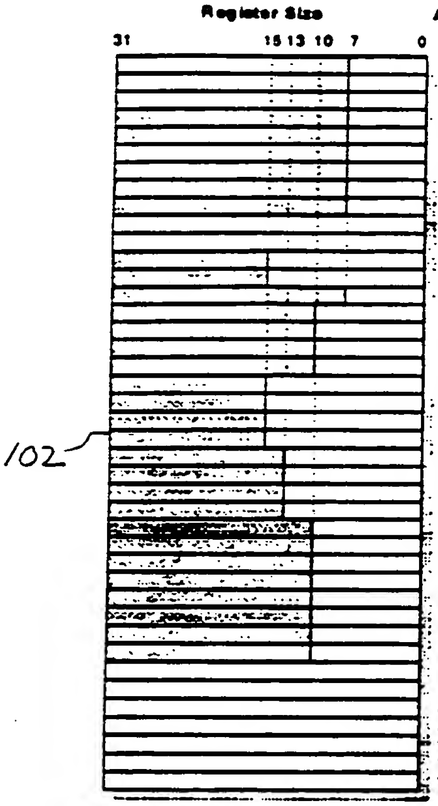
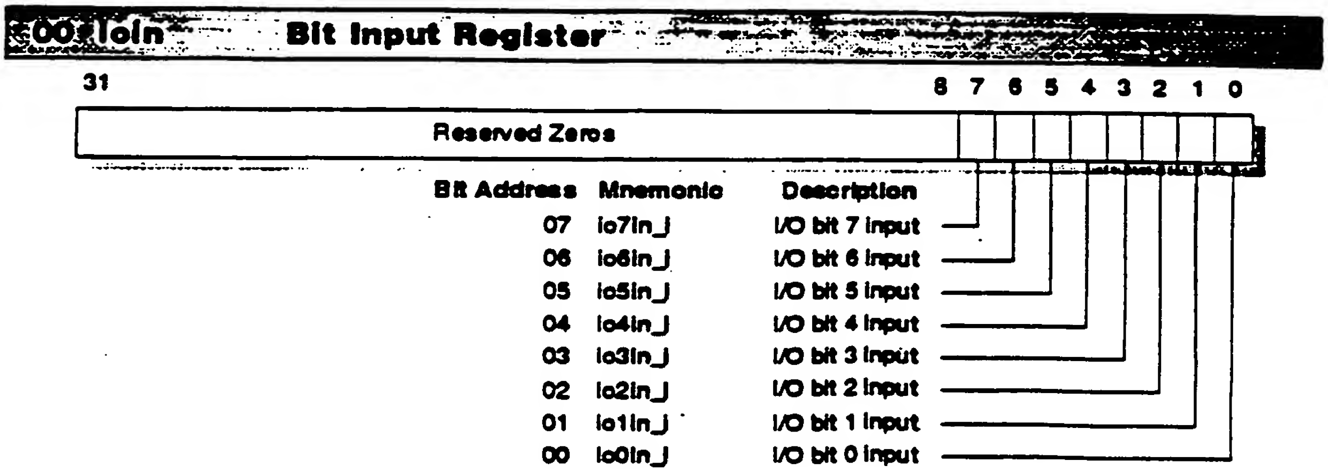


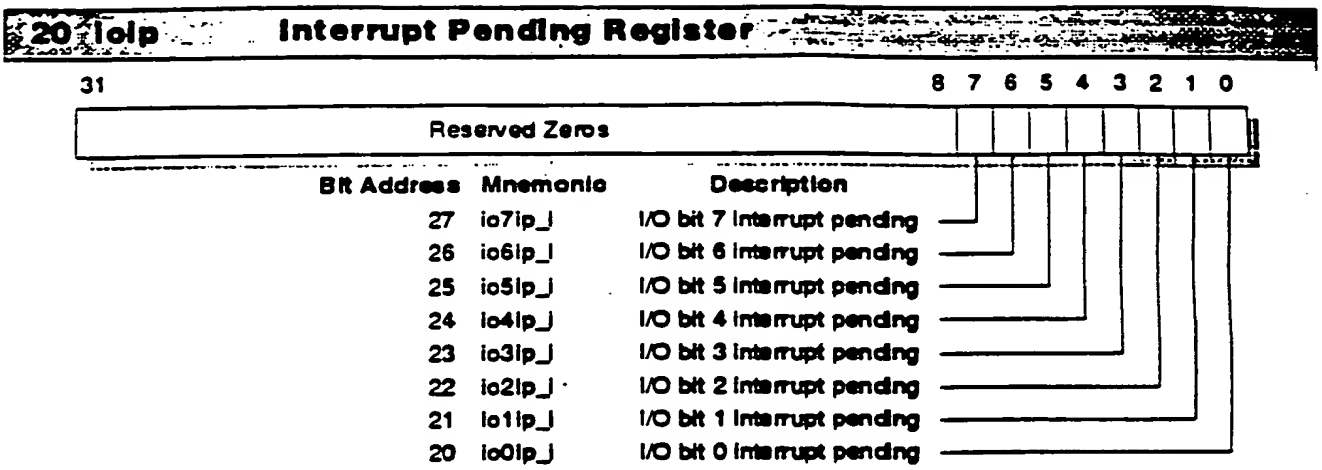
| Addr | Mnemonic | Description |
|---|---|---|
| 000 | ioin | Bit Input Register |
| 020 | ioip | Interrupt Pending Register |
| 040 | ioius | Interrupt Under Service Register |
| 060 | ioout | Bit Output Register |
| 080 | ioie | Interrupt Enable Register |
| 0a0 | iodmae | DMA Enable Register |
| 0c0 | vram | VRAM Control Bit Register |
| 0e0 | misca | Miscellaneous A Register |
| 100 | miscb | Miscellaneous B Register |
| 120 | mfltaddr | Memory Fault Address Register |
| 140 | mfltdata | Memory Fault Data Register |
| 160 | msgsm | Memory System Group Select Mask Register |
| 180 | mgds | Memory Group Device Size Register |
| 1a0 | miscc | Miscellaneous C Register |
| 1c0 | mg0ebt | Memory Group 0 Extended Bus Timing Register |
| 1e0 | mg1ebt | Memory Group 1 Extended Bus Timing Register |
| 200 | mg2ebt | Memory Group 2 Extended Bus Timing Register |
| 220 | mg3ebt | Memory Group 3 Extended Bus Timing Register |
| 240 | mg0casbt | Memory Group 0 CAS Bus Timing Register |
| 260 | mg1casbt | Memory Group 1 CAS Bus Timing Register |
| 280 | mg2casbt | Memory Group 2 CAS Bus Timing Register |
| 2a0 | mg3casbt | Memory Group 3 CAS Bus Timing Register |
| 2c0 | mg0rasbt | Memory Group 0 RAS Bus Timing Register |
| 2e0 | mg1rasbt | Memory Group 1 RAS Bus Timing Register |
| 300 | mg2rasbt | Memory Group 2 RAS Bus Timing Register |
| 320 | mg3rasbt | Memory Group 3 RAS Bus Timing Register |
| 340 | io0ebt | I/O Channel 0 Extended Bus Timing Register |
| 360 | io1ebt | I/O Channel 1 Extended Bus Timing Register |
| 380 | io2ebt | I/O Channel 2 Extended Bus Timing Register |
| 3a0 | io3ebt | I/O Channel 3 Extended Bus Timing Register |
| 3c0 | io4ebt | I/O Channel 4 Extended Bus Timing Register |
| 3e0 | io5ebt | I/O Channel 5 Extended Bus Timing Register |
| 400 | io6ebt | I/O Channel 6 Extended Bus Timing Register |
| 420 | io7ebt | I/O Channel 7 Extended Bus Timing Register |
| 440 | msra | Memory System Refresh Address Register (WO) |
| 440 | iopdelay | IOP Delay Register (RO) |
| 460 | iodtta | I/O Device Transfer Types A Register |
| 480 | iodttb | I/O Device Transfer Types B Register |
| 7a0 | iodmaex | I/O DMA Enable Expiration Register |
| 7c0 | drivers | Driver Current Register |
| 7e0 | iopreset | IOP Reset Register |

FIG. 20



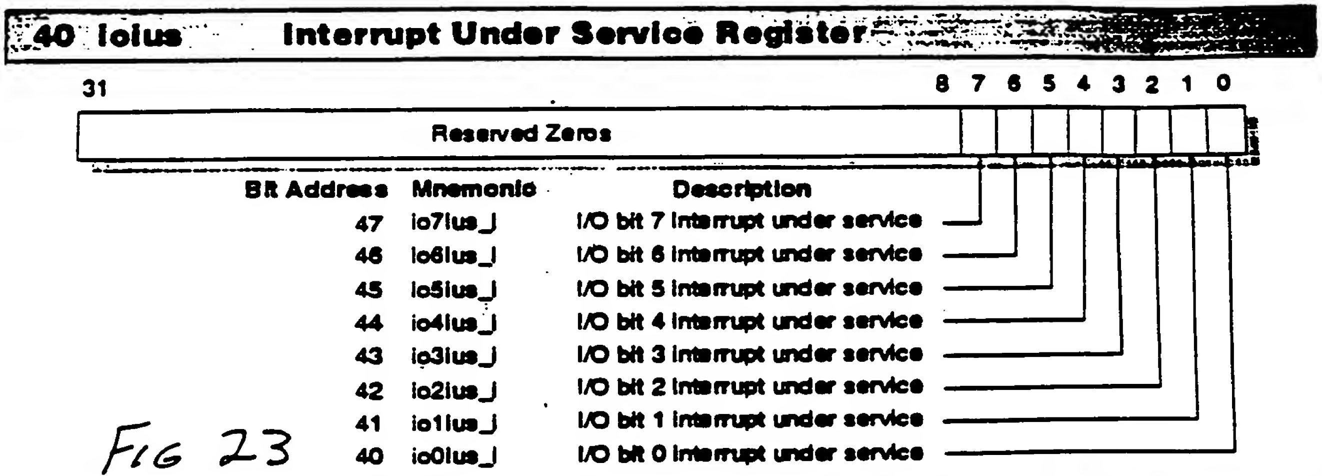
| Bit Address | Mnemonic | Description |
|---|---|---|
| 07 | io7in_l | I/O bit 7 input |
| 06 | io6in_l | I/O bit 6 input |
| 05 | io5in_l | I/O bit 5 input |
| 04 | io4in_l | I/O bit 4 input |
| 03 | io3in_l | I/O bit 3 input |
| 02 | io2in_l | I/O bit 2 input |
| 01 | io1in_l | I/O bit 1 input |
| 00 | io0in_l | I/O bit 0 input |

FIG. 21



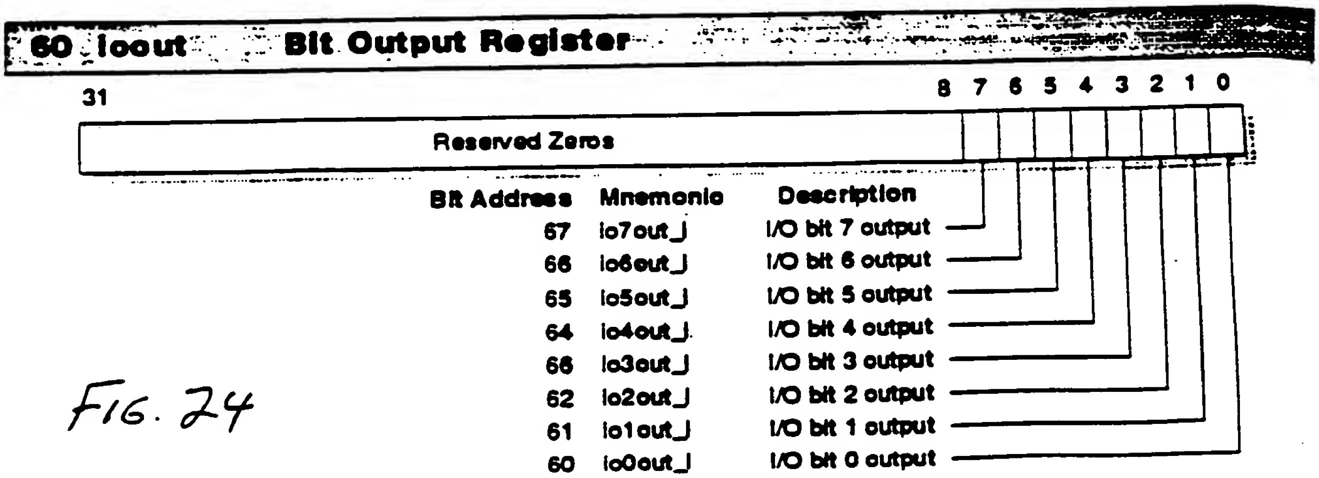
| Bit Address | Mnemonic | Description |
|---|---|---|
| 27 | io7ip_l | I/O bit 7 interrupt pending |
| 26 | io6ip_l | I/O bit 6 interrupt pending |
| 25 | io5ip_l | I/O bit 5 interrupt pending |
| 24 | io4ip_l | I/O bit 4 interrupt pending |
| 23 | io3ip_l | I/O bit 3 interrupt pending |
| 22 | io2ip_l | I/O bit 2 interrupt pending |
| 21 | io1ip_l | I/O bit 1 interrupt pending |
| 20 | io0ip_l | I/O bit 0 interrupt pending |

FIG. 22



| Bit Address | Mnemonic | Description |
|---|---|---|
| 47 | io7ius_l | I/O bit 7 interrupt under service |
| 46 | io6ius_l | I/O bit 6 interrupt under service |
| 45 | io5ius_l | I/O bit 5 interrupt under service |
| 44 | io4ius_l | I/O bit 4 interrupt under service |
| 43 | io3ius_l | I/O bit 3 interrupt under service |
| 42 | io2ius_l | I/O bit 2 interrupt under service |
| 41 | io1ius_l | I/O bit 1 interrupt under service |
| 40 | io0ius_l | I/O bit 0 interrupt under service |

FIG 23



| Bit Address | Mnemonic | Description |
|---|---|---|
| 67 | io7out_l | I/O bit 7 output |
| 66 | io6out_l | I/O bit 6 output |
| 65 | io5out_l | I/O bit 5 output |
| 64 | io4out_l | I/O bit 4 output |
| 63 | io3out_l | I/O bit 3 output |
| 62 | io2out_l | I/O bit 2 output |
| 61 | io1out_l | I/O bit 1 output |
| 60 | io0out_l | I/O bit 0 output |

FIG. 24

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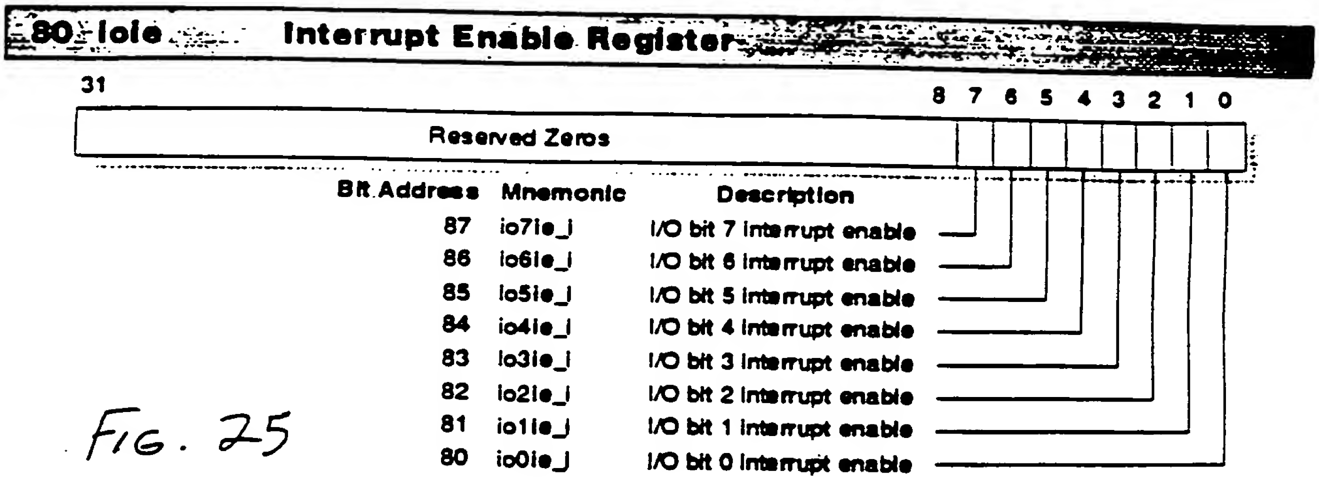

FIG. 25

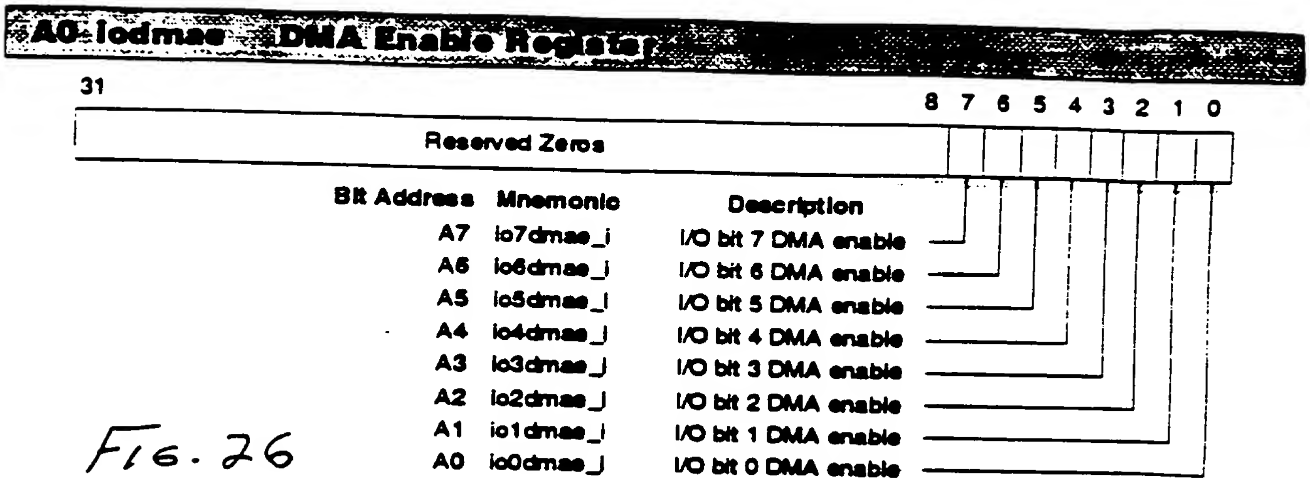

FIG. 26

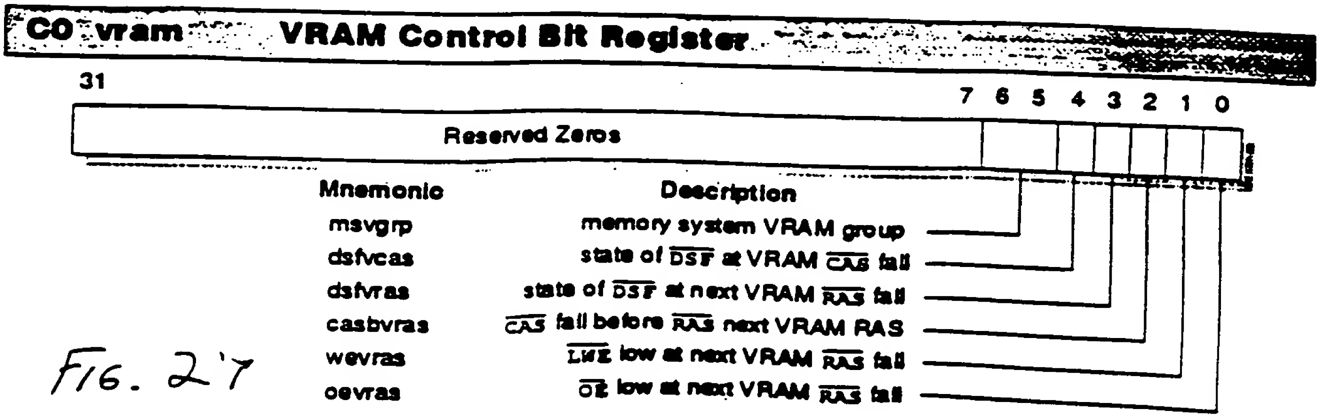

FIG. 27

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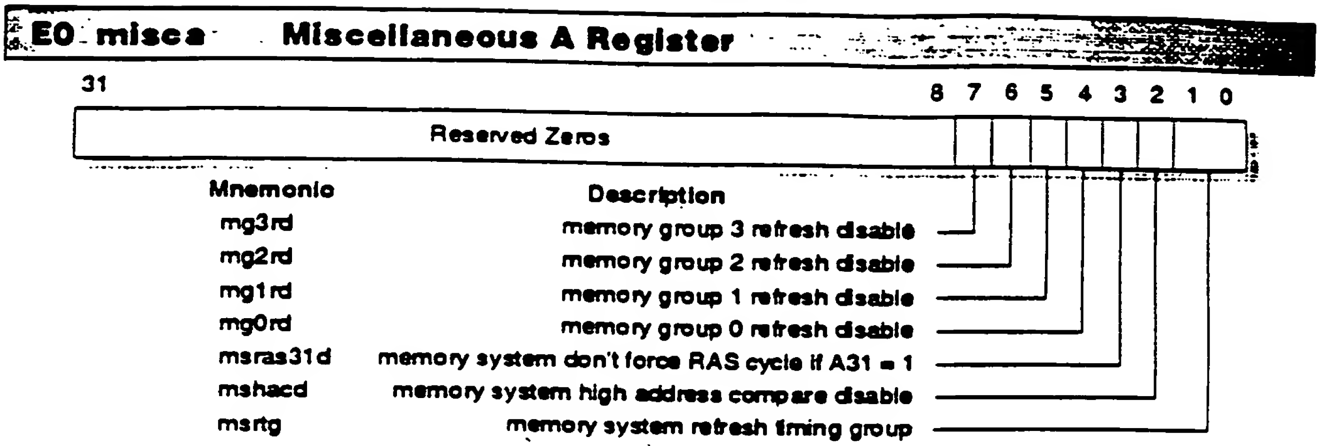
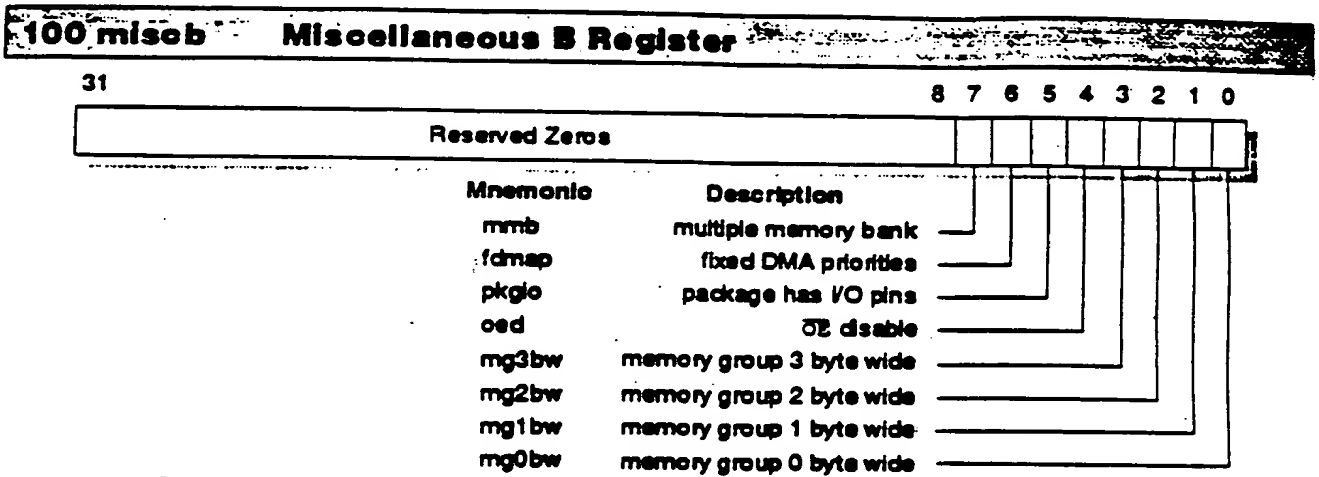
**E0 misca Miscellaneous A Register**



| Mnemonic | Description |
|---|---|
| mg3rd | memory group 3 refresh disable |
| mg2rd | memory group 2 refresh disable |
| mg1rd | memory group 1 refresh disable |
| mg0rd | memory group 0 refresh disable |
| msras31d | memory system don't force RAS cycle if A31 = 1 |
| mshacd | memory system high address compare disable |
| msrtg | memory system refresh timing group |

FIG. 28

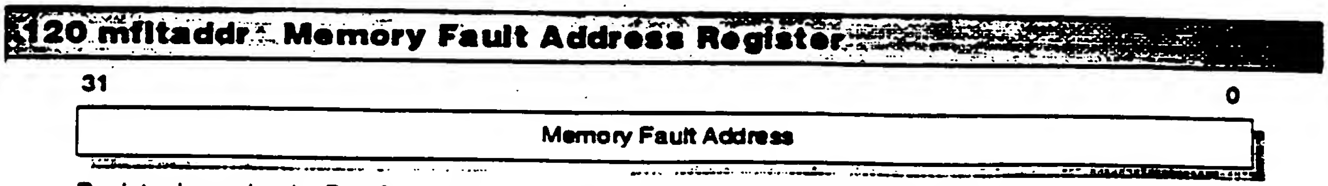
**100 miscb Miscellaneous B Register**



| Mnemonic | Description |
|---|---|
| mmb | multiple memory bank |
| fdmap | fixed DMA priorities |
| pkgio | package has I/O pins |
| oed | $\overline{OE}$ disable |
| mg3bw | memory group 3 byte wide |
| mg2bw | memory group 2 byte wide |
| mg1bw | memory group 1 byte wide |
| mg0bw | memory group 0 byte wide |

FIG. 29

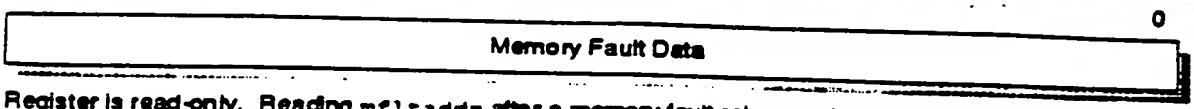
**120 mfltaddr Memory Fault Address Register**



Register is read-only. Reading `mfltaddr` after a memory fault releases the data lock on `mfltaddr` and `mfltdata`, allowing data to flow into the registers.

FIG. 30

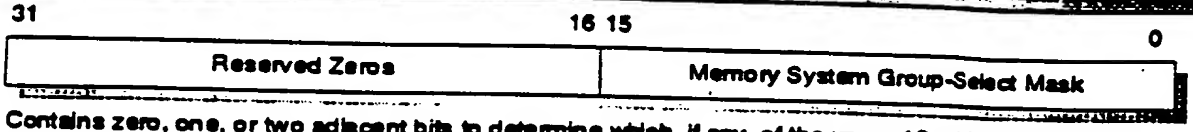
## 140 mfltdata Memory Fault Data Register



Register is read-only. Reading `mfltaddr` after a memory fault releases the data lock on `mfltaddr` and `mfltdata`, allowing data to flow into the registers.

FIG. 31

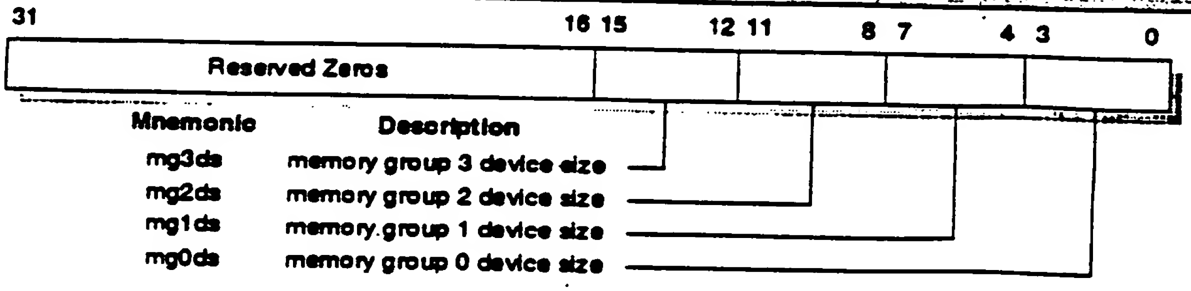
## 160 msgsm Memory System Group Select Mask Register



Contains zero, one, or two adjacent bits to determine which, if any, of the upper 16 address bits will be decoded to select memory groups.

FIG. 32

## 180 mgds Memory Group Device Size Register



| Mnemonic | Description |
|---|---|
| mg3ds | memory group 3 device size |
| mg2ds | memory group 2 device size |
| mg1ds | memory group 1 device size |
| mg0ds | memory group 0 device size |

Device Sizes

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0x00 | 64K DRAM | 0x04 | 1M DRAM | 0x08 | 8M DRAM | 0x0c | 64M DRAM (asym) |
| 0x01 | 128K DRAM | 0x05 | 2M DRAM | 0x09 | 16M DRAM (asym) | 0x0d | 64M DRAM |
| 0x02 | 256K DRAM | 0x06 | 4M DRAM (asym) | 0x0a | 16M DRAM | 0x0e | 128M DRAM |
| 0x03 | 512K DRAM | 0x07 | 4M DRAM | 0x0b | 32M DRAM | 0x0f | SRAM |

FIG. 33

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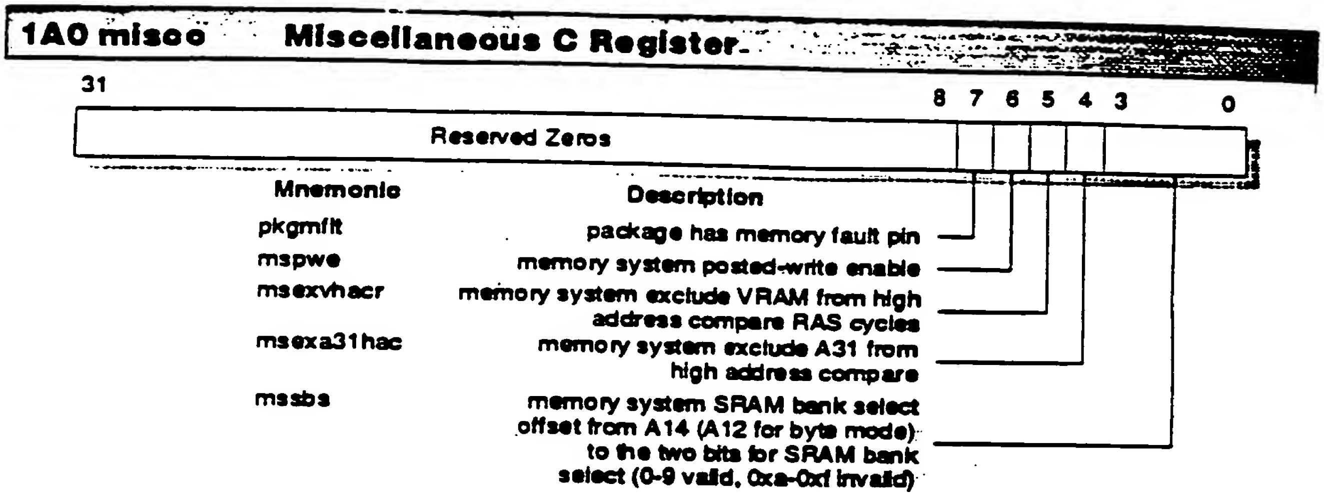

FIG. 34

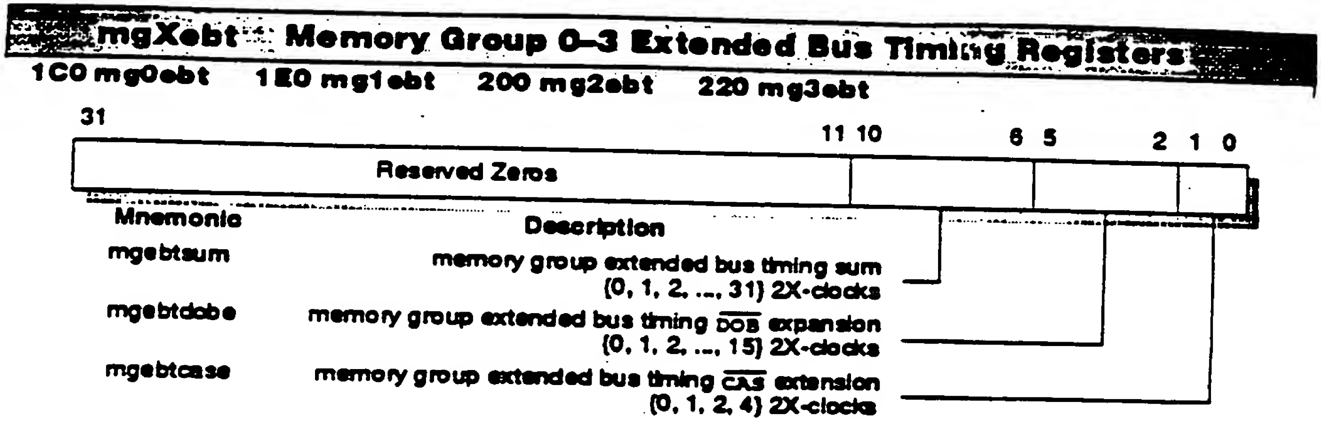

FIG. 35

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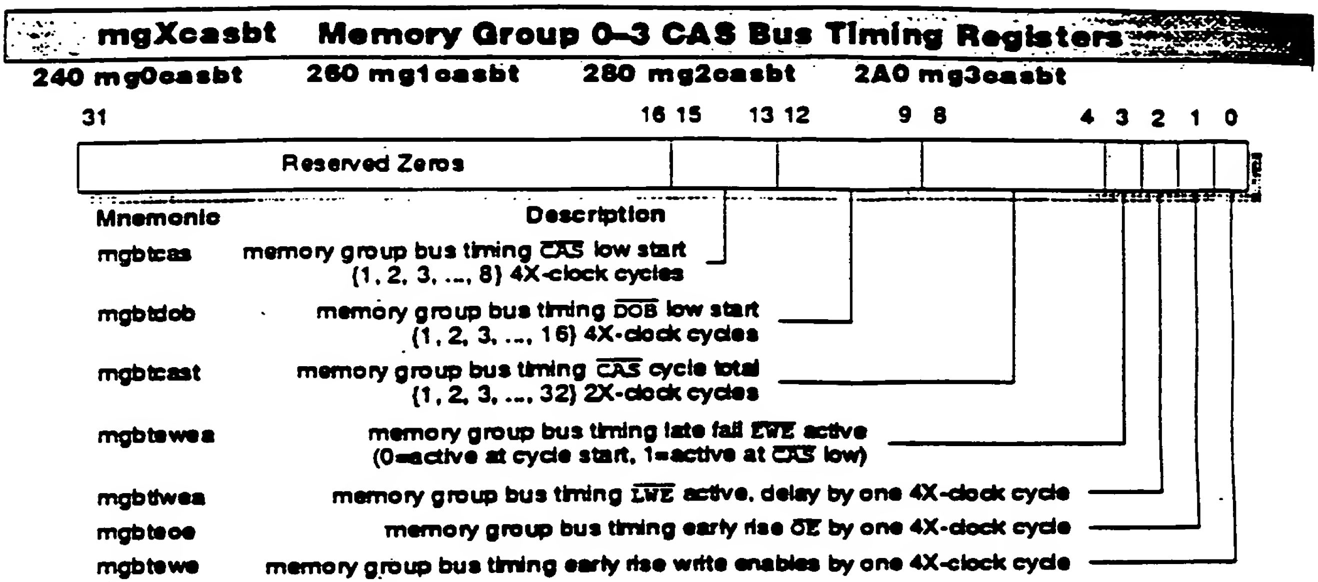

FIG. 36

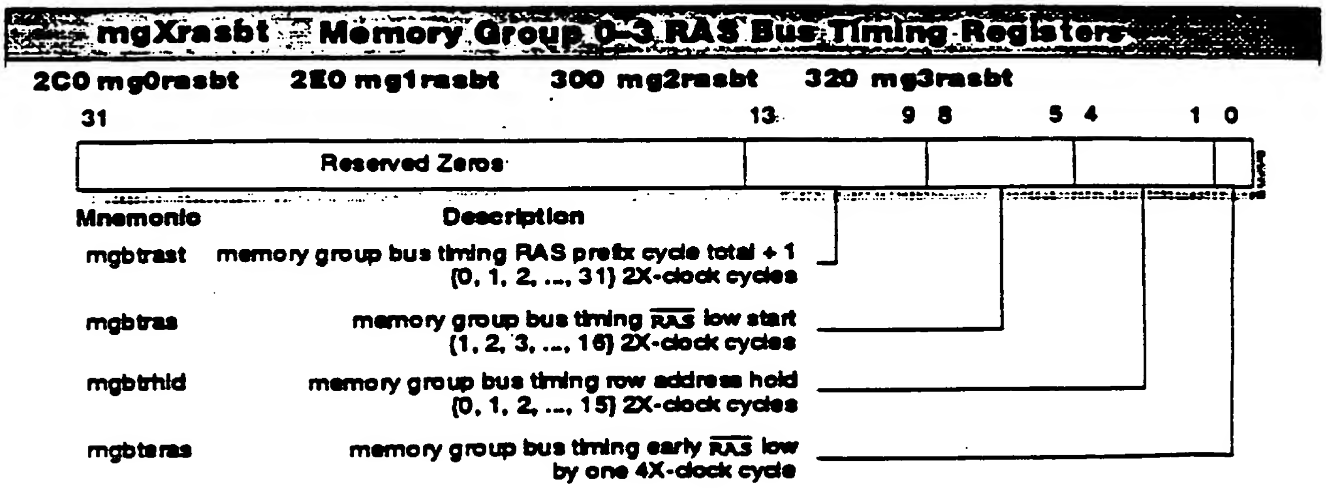

FIG. 37

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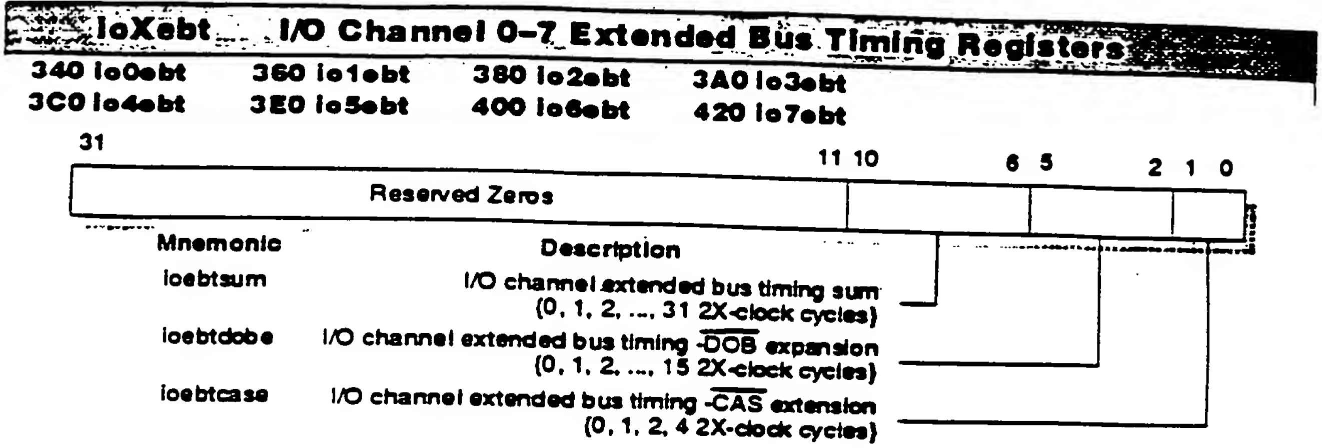

FIG. 38

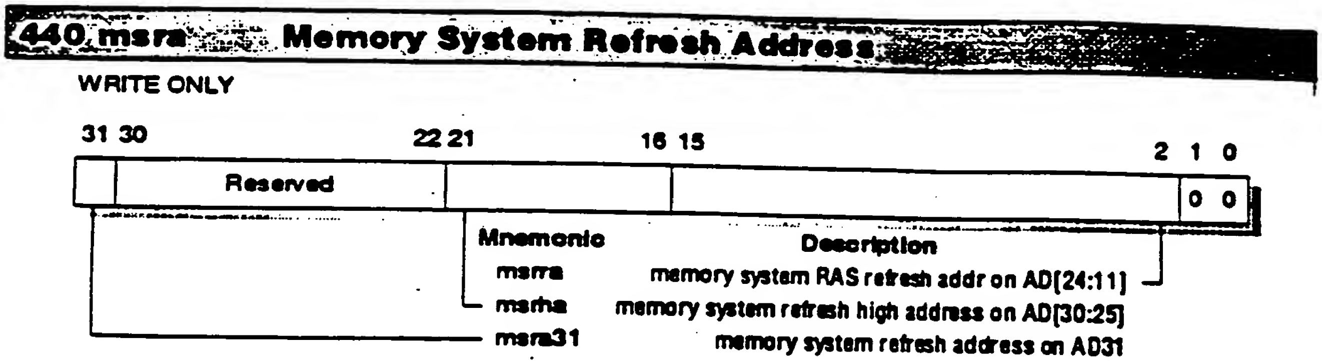

FIG. 39

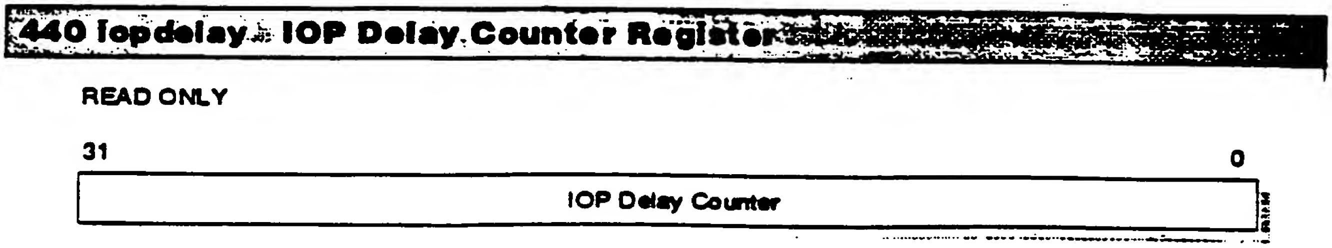

FIG. 40

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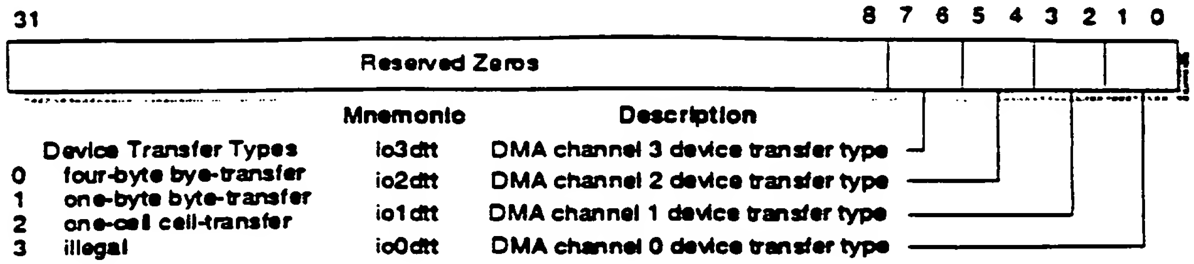
## 460 iodtta I/O Device Transfer Types A Register



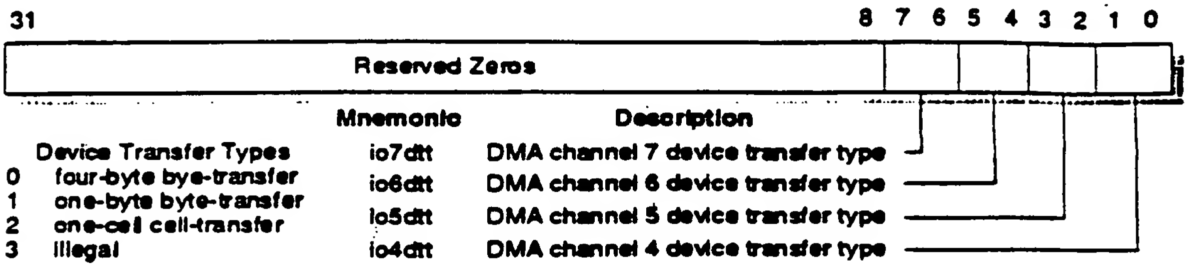
| Mnemonic | Description |
|---|---|
| io3dtt | DMA channel 3 device transfer type |
| io2dtt | DMA channel 2 device transfer type |
| io1dtt | DMA channel 1 device transfer type |
| io0dtt | DMA channel 0 device transfer type |

Device Transfer Types

| | |
|---|---|
| 0 | four-byte bye-transfer |
| 1 | one-byte byte-transfer |
| 2 | one-cel cell-transfer |
| 3 | illegal |

FIG. 41

## 480 iodttb I/O Device Transfer Types B Register



| Mnemonic | Description |
|---|---|
| io7dtt | DMA channel 7 device transfer type |
| io6dtt | DMA channel 6 device transfer type |
| io5dtt | DMA channel 5 device transfer type |
| io4dtt | DMA channel 4 device transfer type |

Device Transfer Types

| | |
|---|---|
| 0 | four-byte bye-transfer |
| 1 | one-byte byte-transfer |
| 2 | one-cel cell-transfer |
| 3 | illegal |

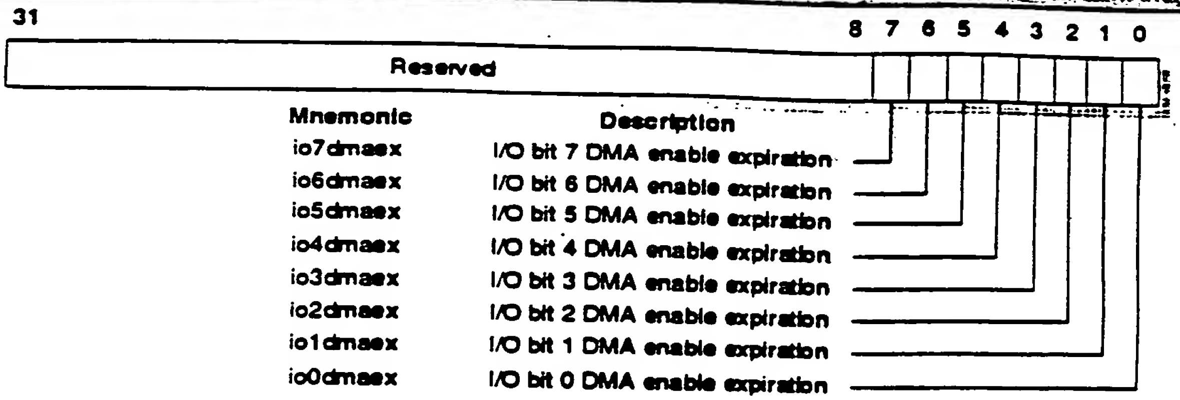
FIG. 42

## Reserved Register Addresses

4A0-780

FIG. 43

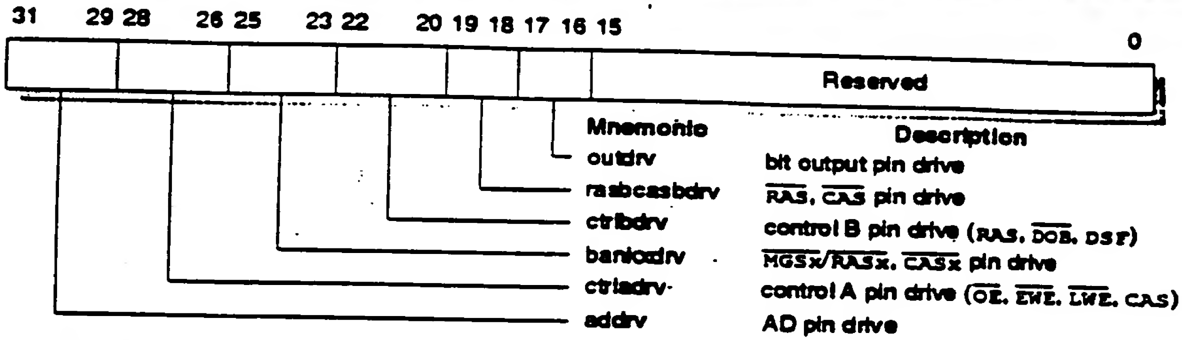
## 7A0 iodmaex DMA Enable Expiration Register



| Mnemonic | Description |
|---|---|
| io7dmaex | I/O bit 7 DMA enable expiration |
| io6dmaex | I/O bit 6 DMA enable expiration |
| io5dmaex | I/O bit 5 DMA enable expiration |
| io4dmaex | I/O bit 4 DMA enable expiration |
| io3dmaex | I/O bit 3 DMA enable expiration |
| io2dmaex | I/O bit 2 DMA enable expiration |
| io1dmaex | I/O bit 1 DMA enable expiration |
| io0dmaex | I/O bit 0 DMA enable expiration |

FIG 44

## 7C0 drivers Driver Current Register

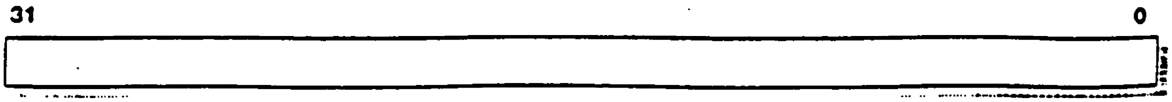


| Mnemonic | Description |
|---|---|
| outdrv | bit output pin drive |
| rasbcasbdrv | $\overline{RAS}$, $\overline{CAS}$ pin drive |
| ctrlbdrv | control B pin drive (RAS, $\overline{DOB}$, DSF) |
| bankdrv | $\overline{MGSx}$/$\overline{RASx}$, $\overline{CASx}$ pin drive |
| ctrladrv | control A pin drive ($\overline{OE}$, $\overline{EWE}$, $\overline{LWE}$, CAS) |
| addrv | AD pin drive |

| 3-Bit Field | | 2-Bit Field | | Where n = | |
|---|---|---|---|---|---|
| 00n | 1 of 3 drivers | 0n | 1 of 3 drivers | 0 | 1 of 2 pre-drivers |
| 01n | 2 of 3 drivers | 1n | 3 of 3 drivers | 1 | 2 of 2 pre-drivers |
| 11n | 3 of 3 drivers | | | | |

FIG. 45

## 7E0 iopreset IOP Reset Register



write reset IOP on any write
read 0xffffffff while waiting to reset, zero otherwise

FIG. 46

FIG 46a

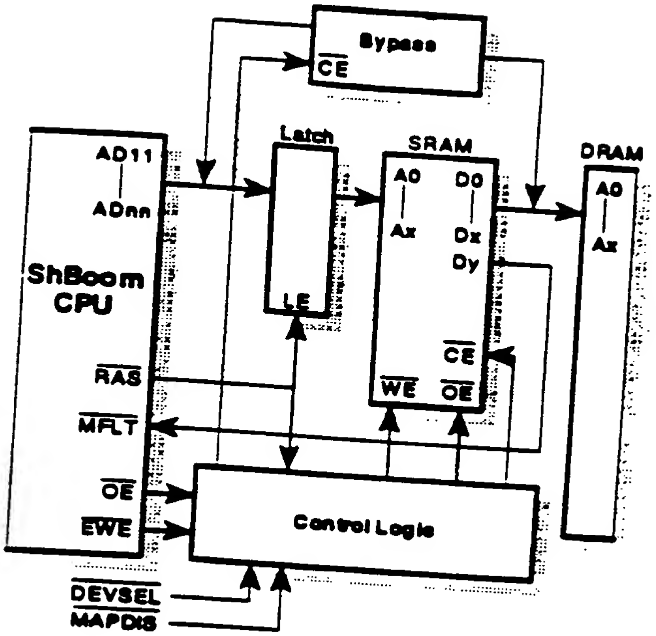
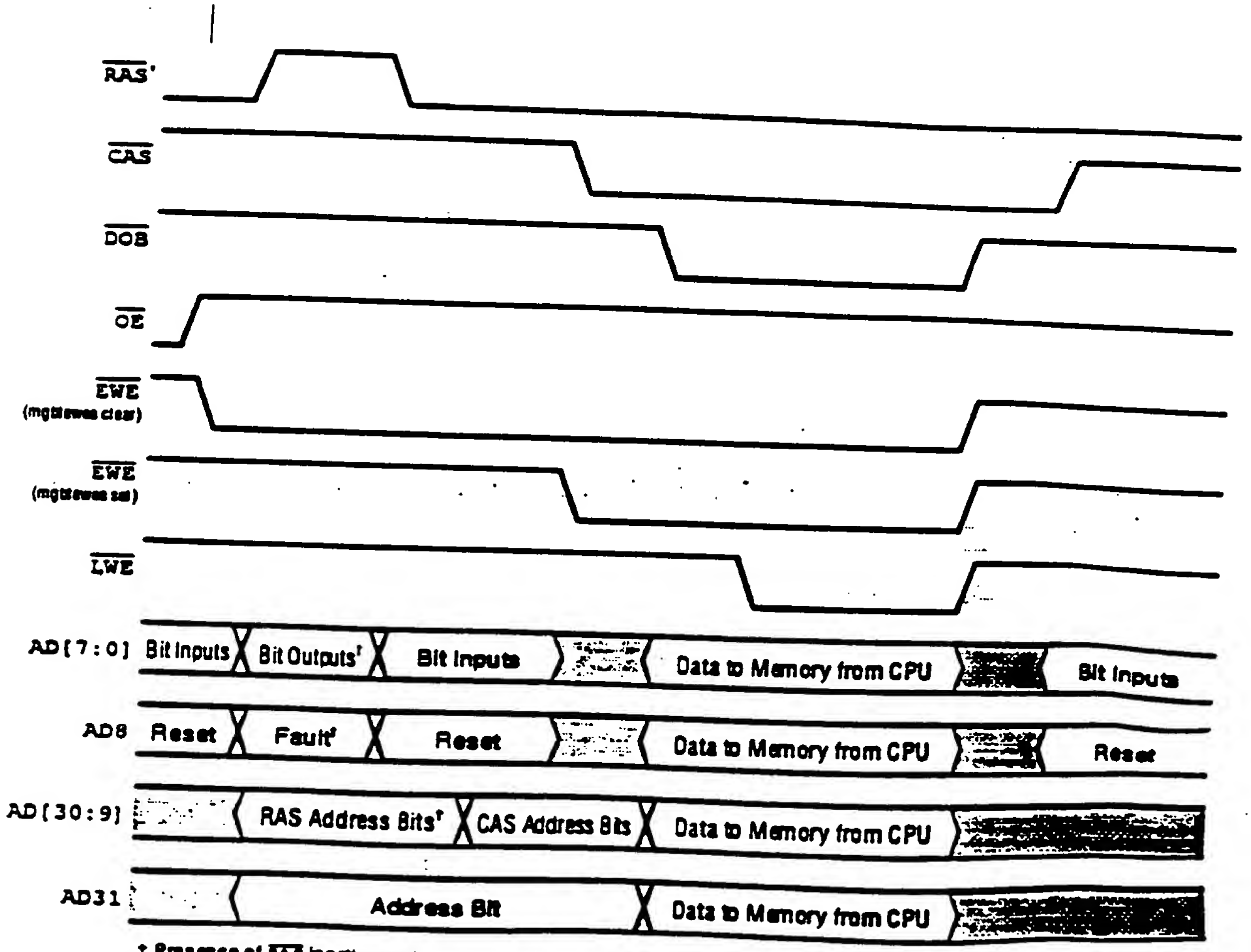


FIG. 47



† Presence of $\overline{RAS}$ inactive period depends on system conditions.

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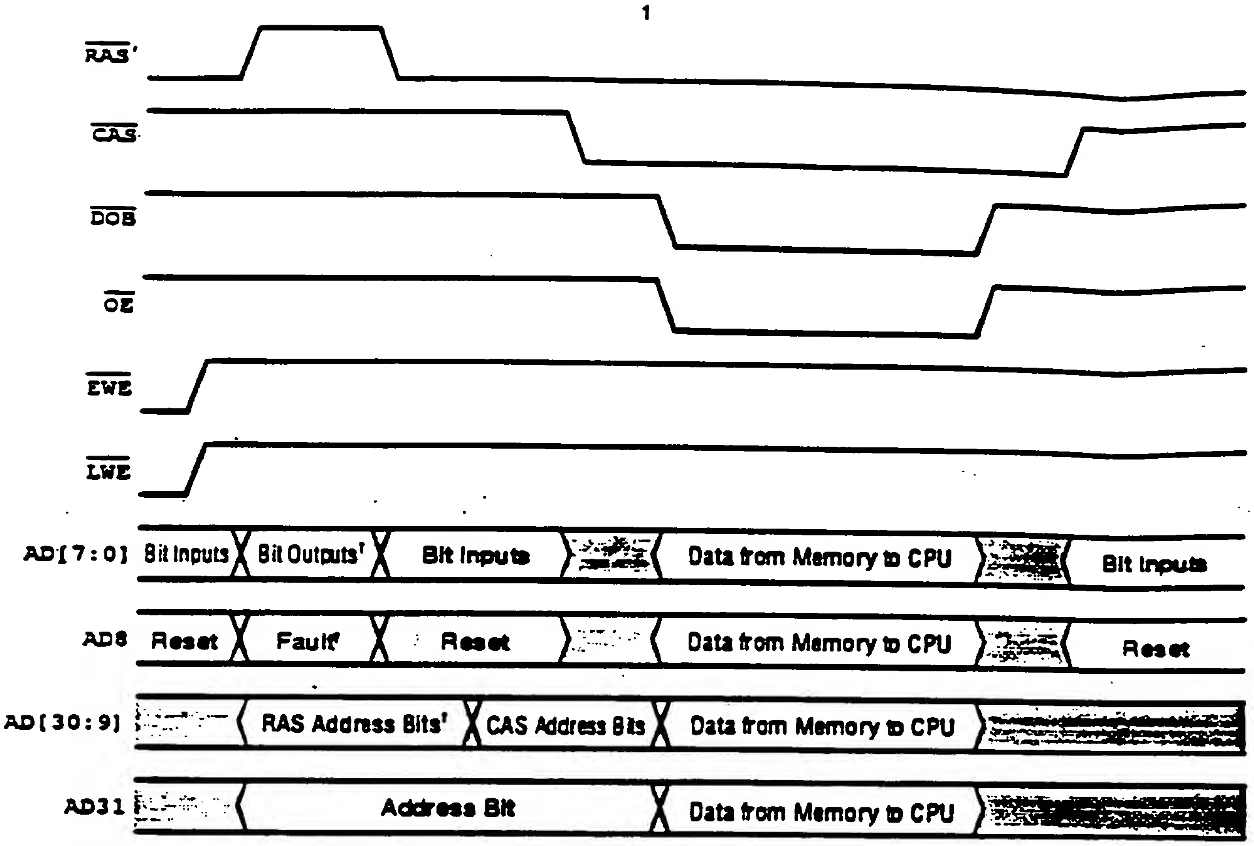

† Presence of $\overline{\text{RAS}}$ inactive period depends on system conditions.

FIG 48

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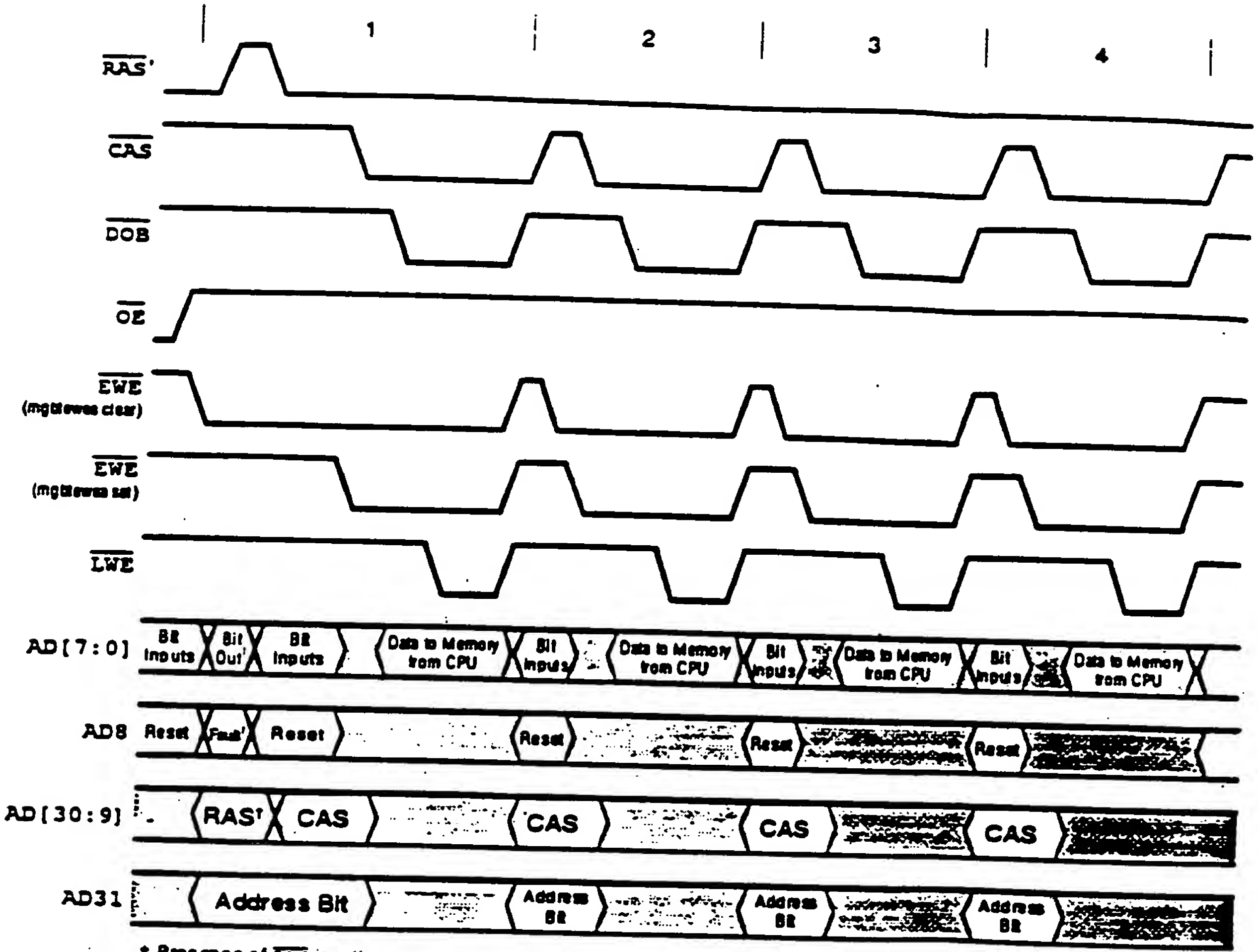

† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 49

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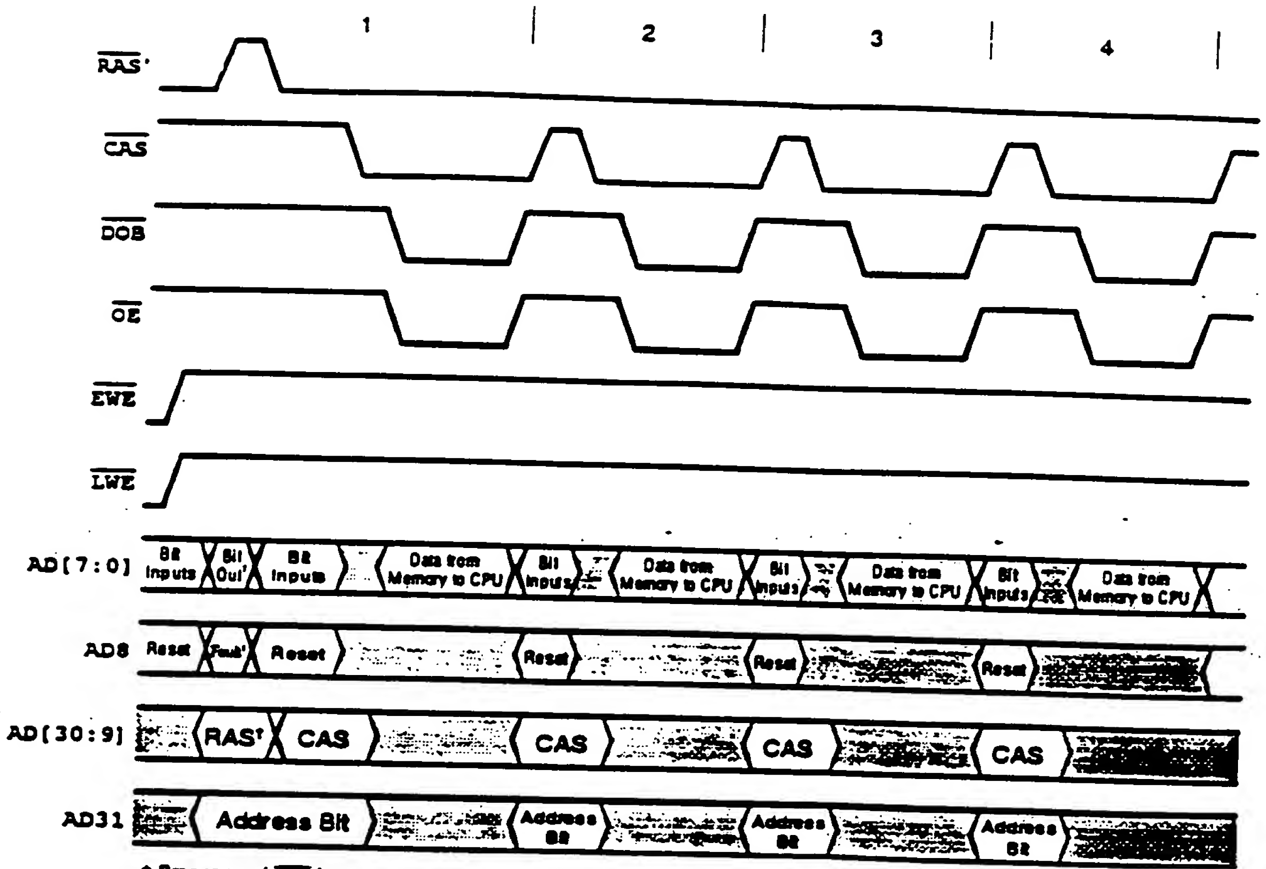

† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 50

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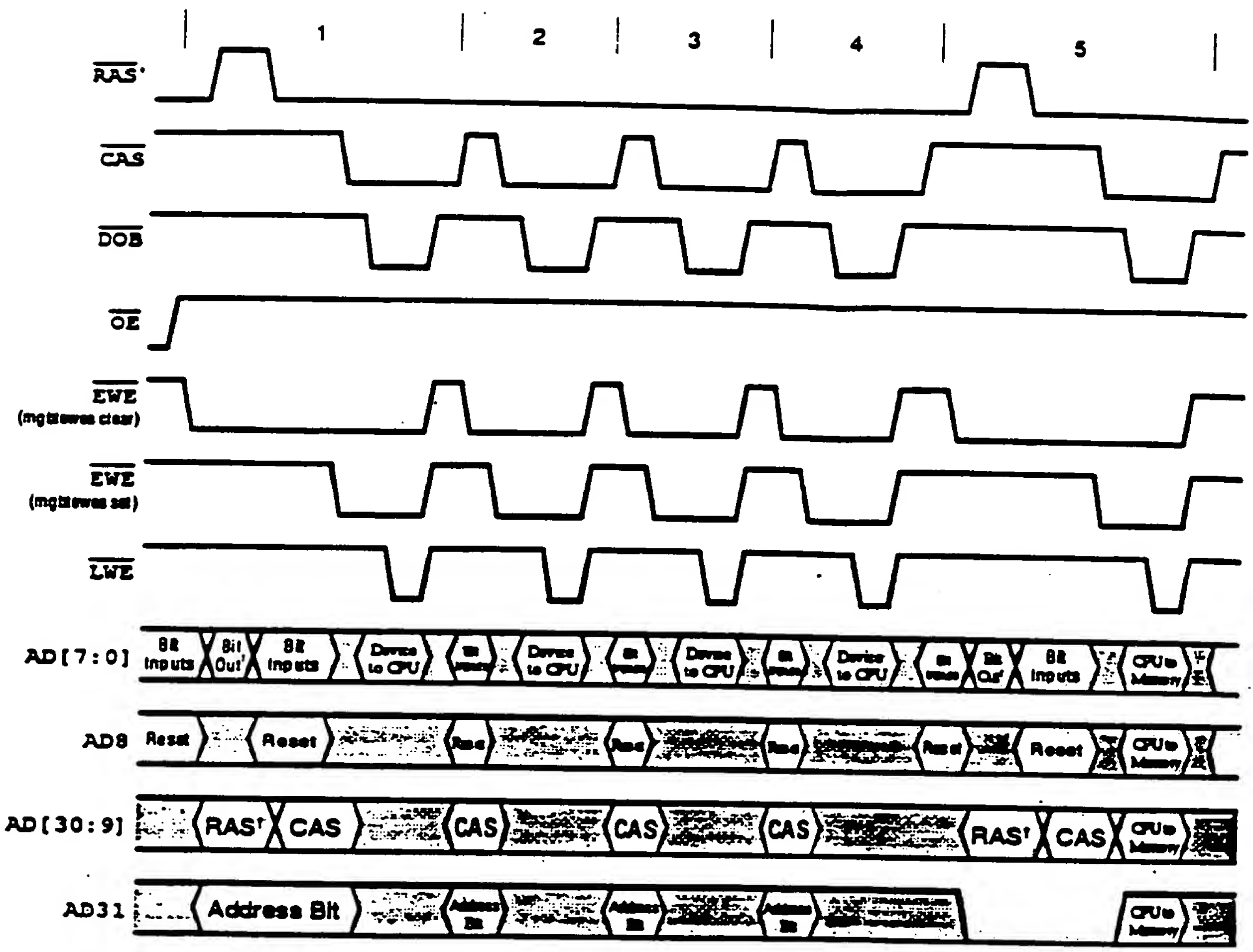

† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 51

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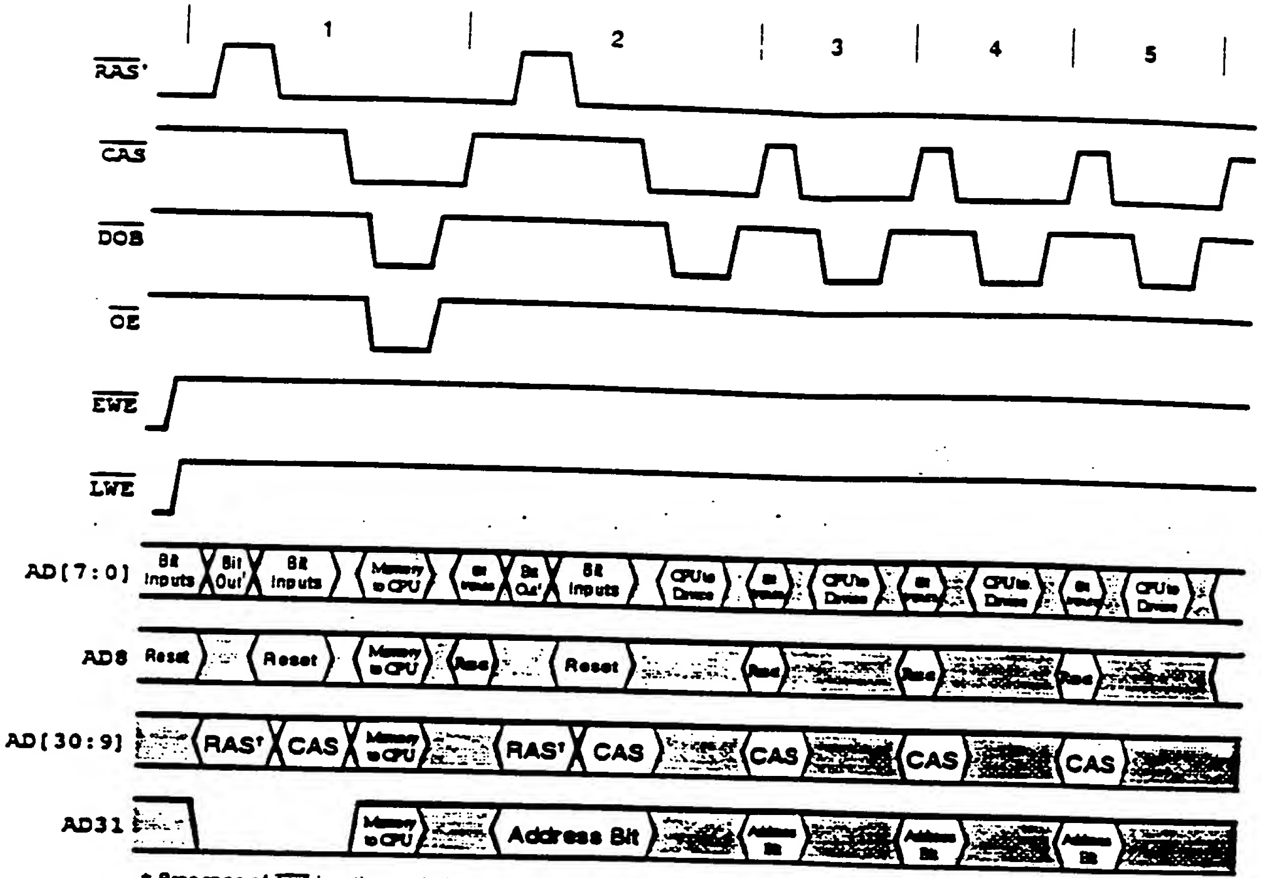

† Presence of RAS inactive period depends on system conditions.

FIG. 52

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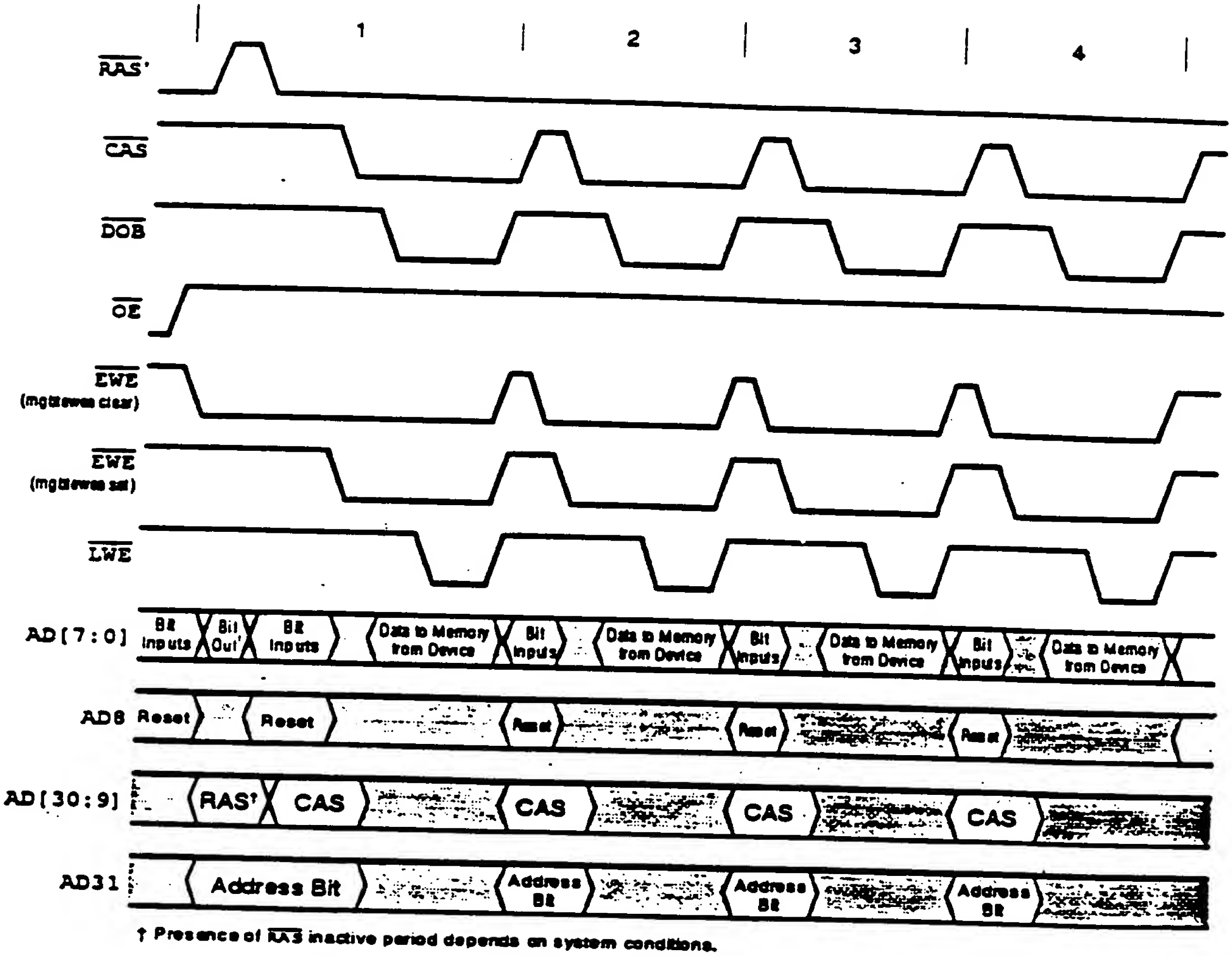

† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 53

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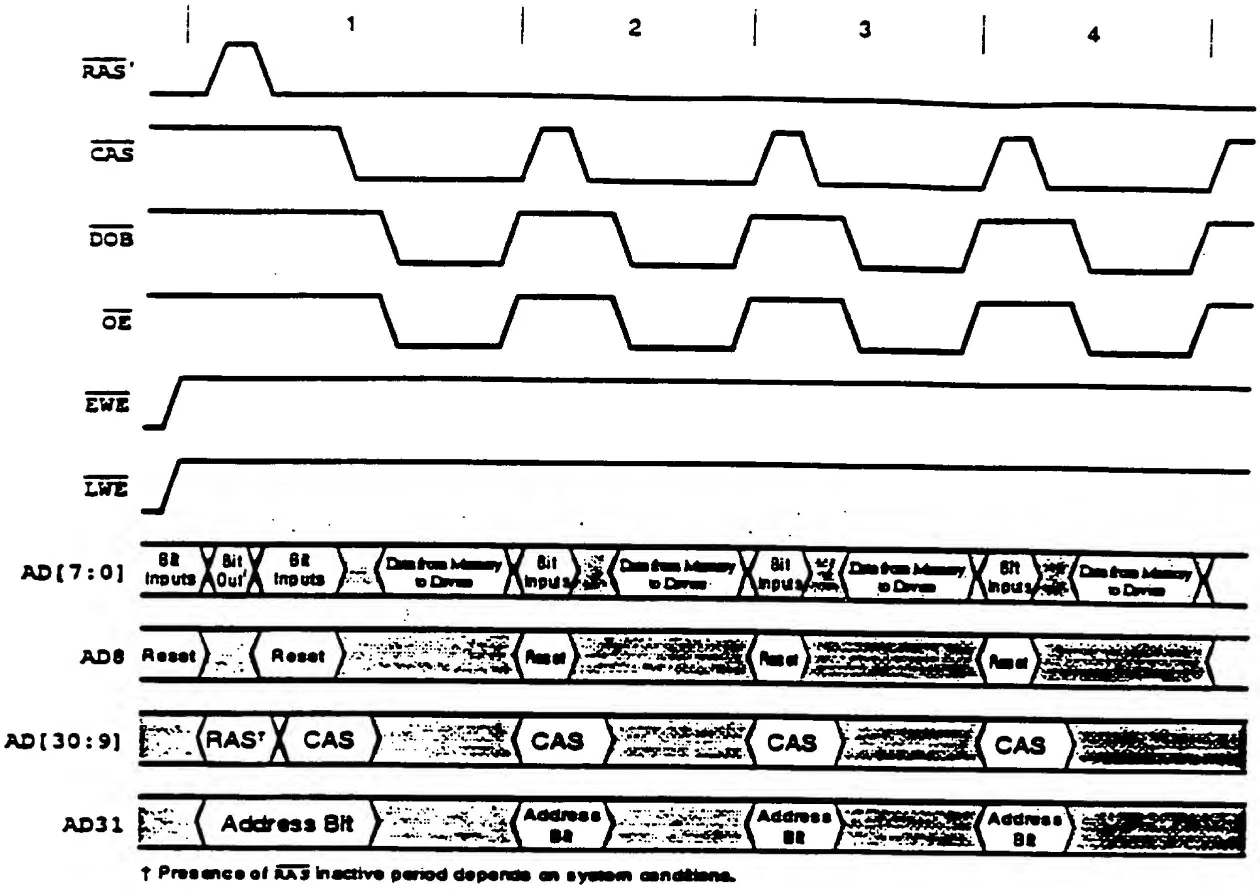
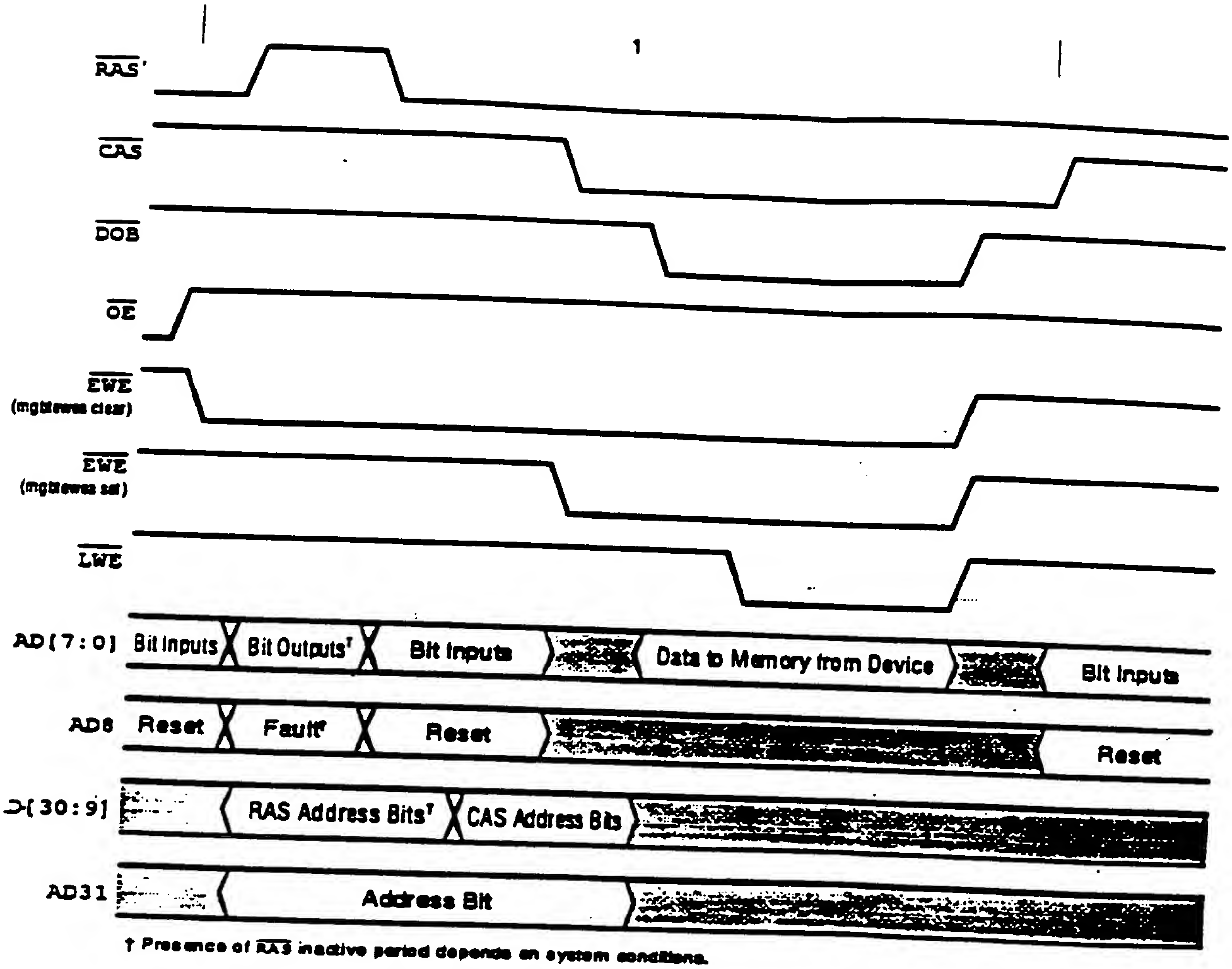


† Presence of RAS inactive period depends on system conditions.

FIG. 54



† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 55

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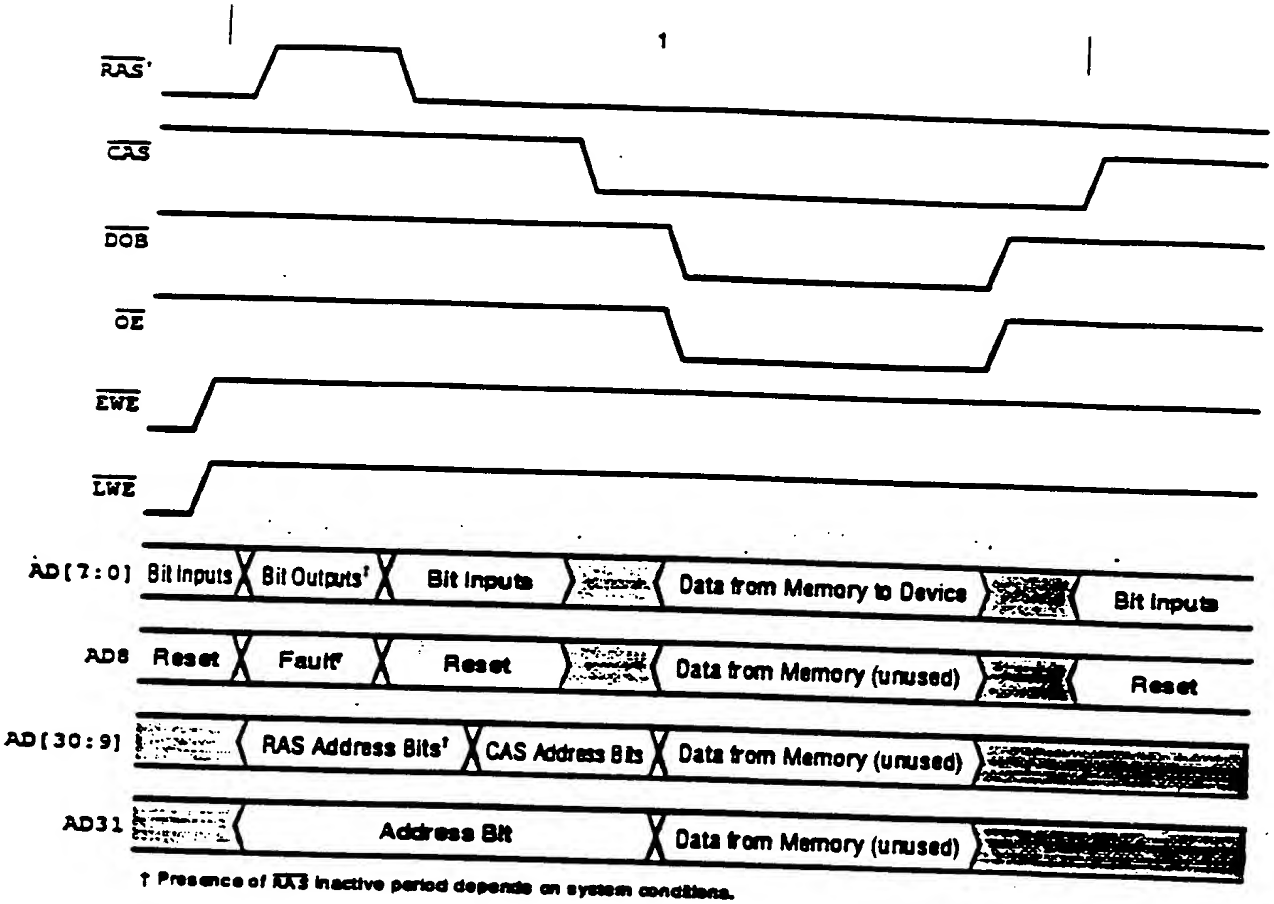
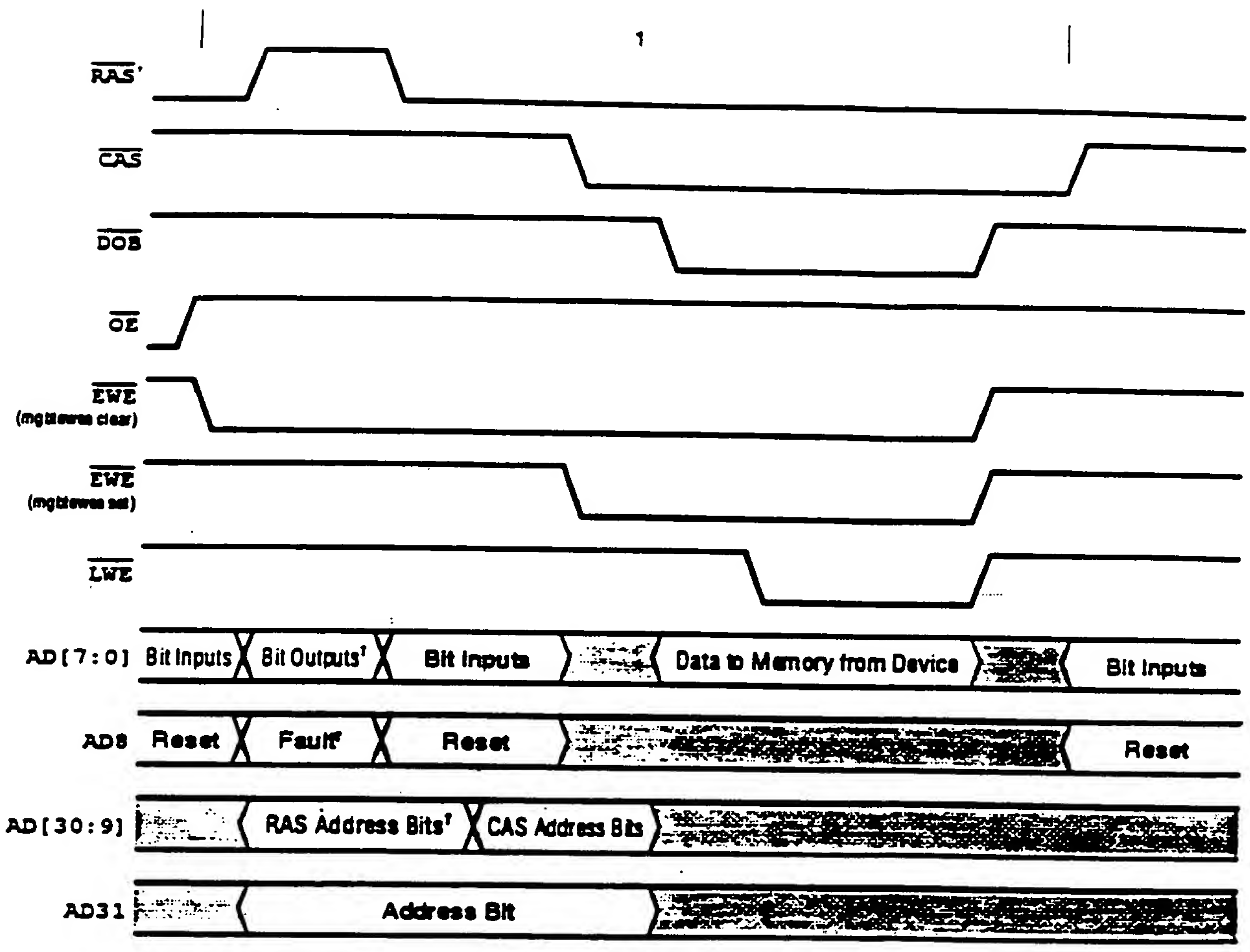


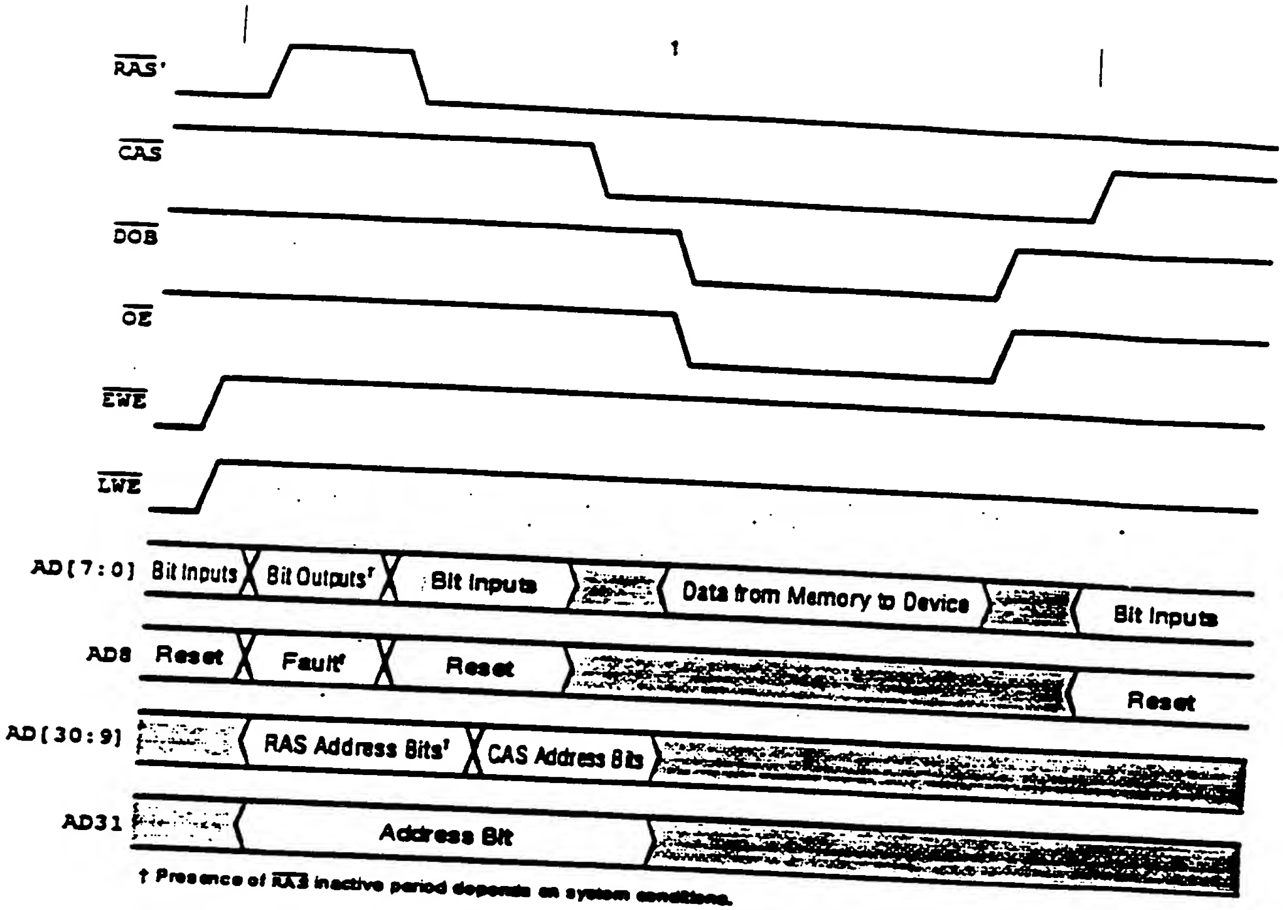
† Presence of RAS inactive period depends on system conditions.

FIG. 56



† Presence of $\overline{\text{RAS}}$ inactive period depends on system conditions.

FIG. 57



† Presence of RAS inactive period depends on system conditions.

FIG. 58

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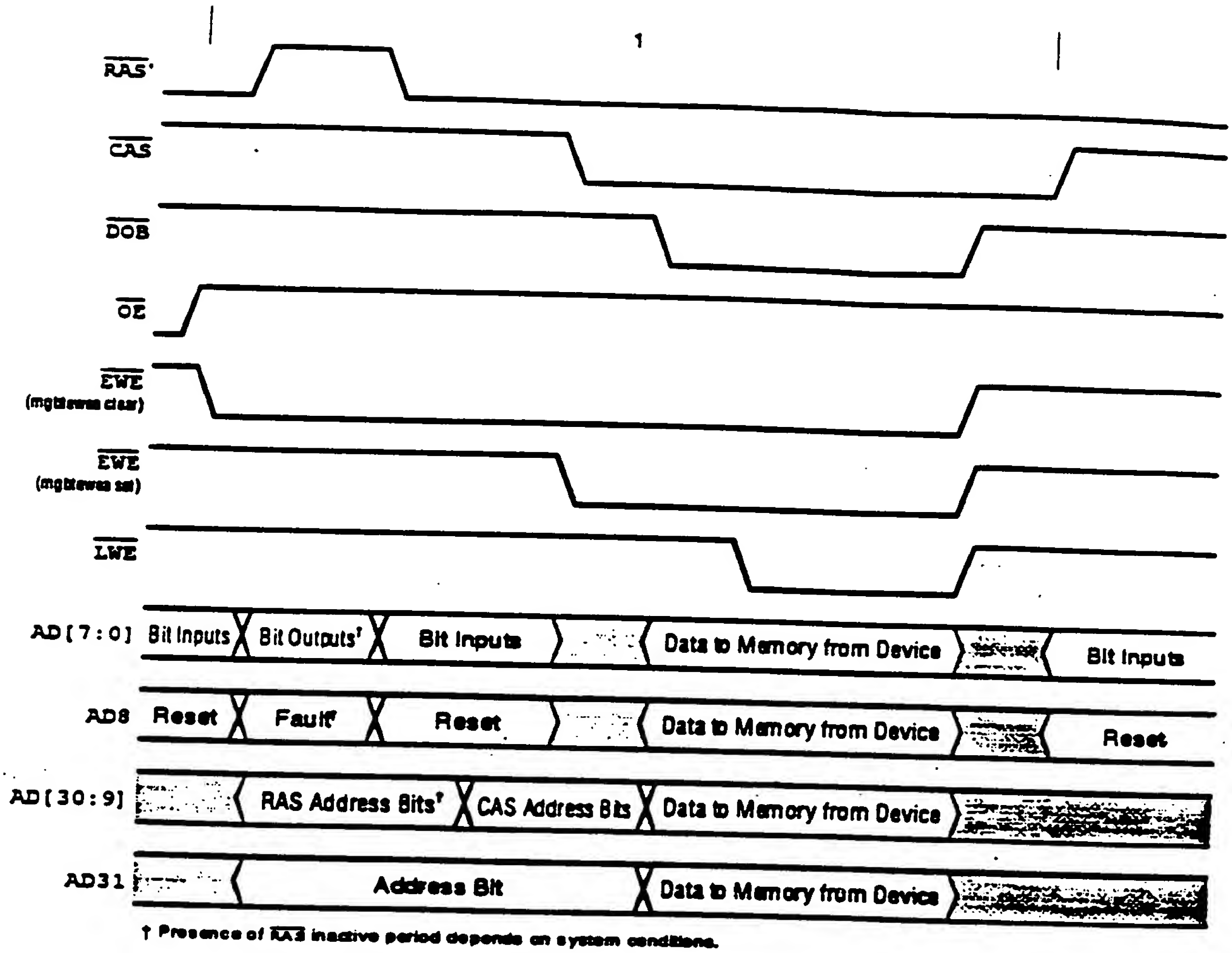

† Presence of $\overline{RAS}$ inactive period depends on system conditions.

FIG. 59

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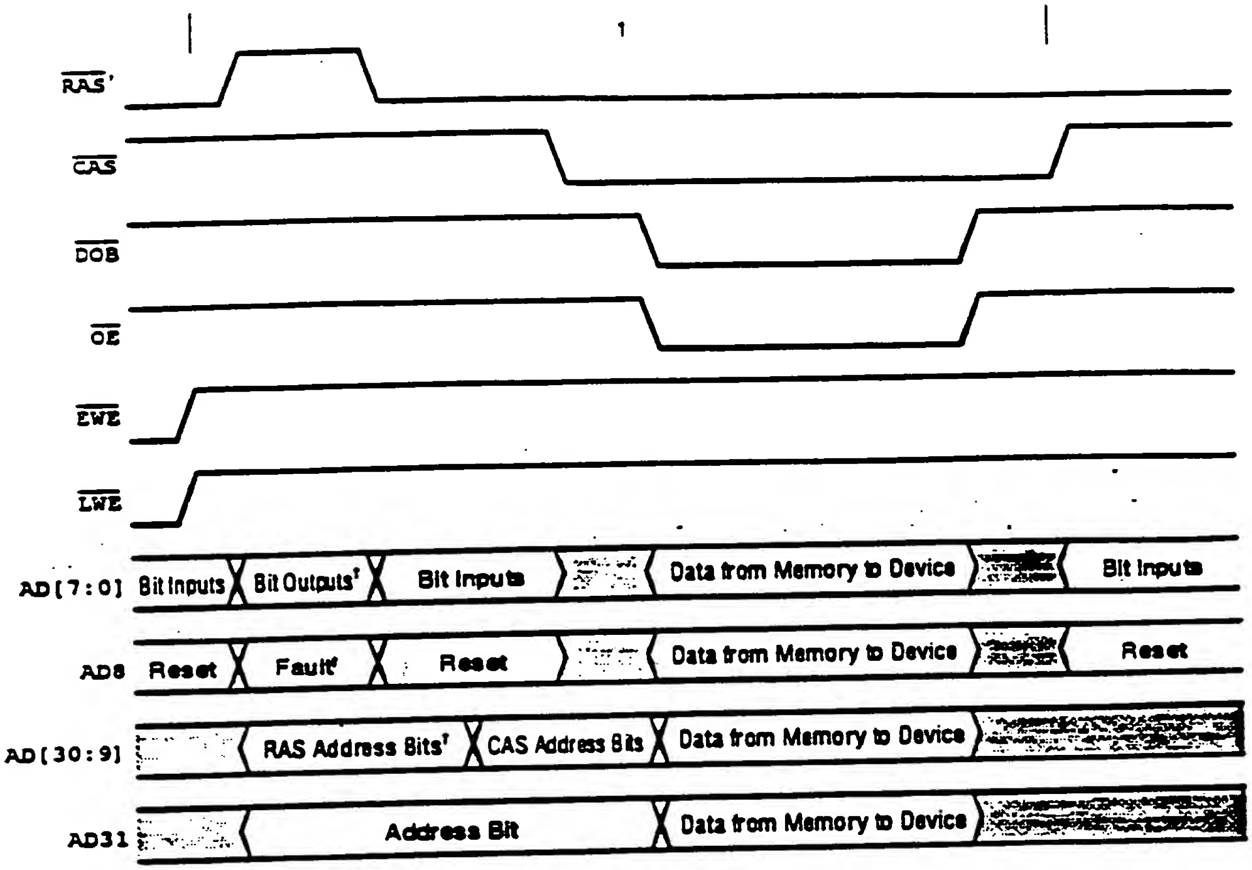

† Presence of RAS inactive period depends on system conditions.

FIG. 60

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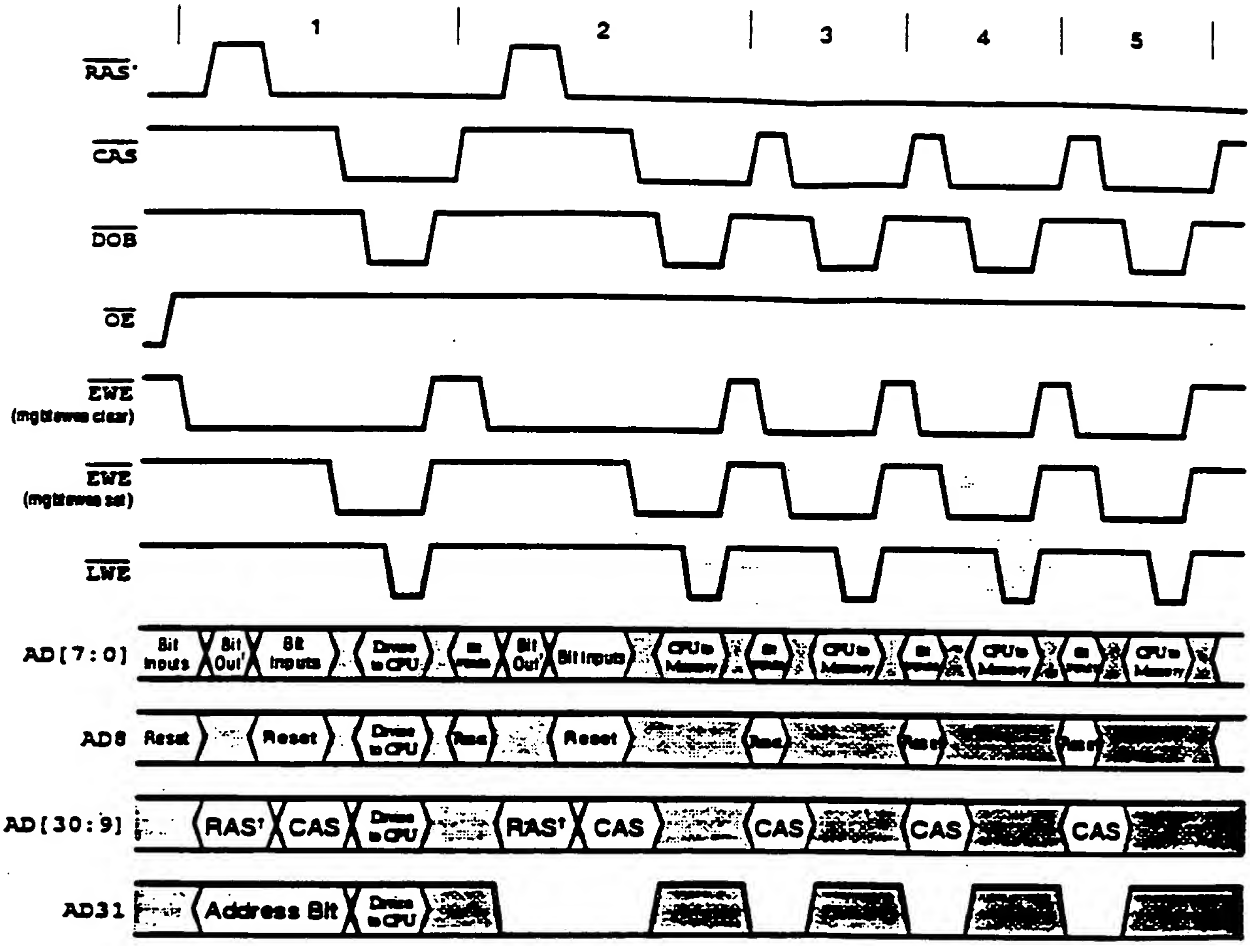

† Presence of RAS inactive period depends on system conditions.

FIG. 61

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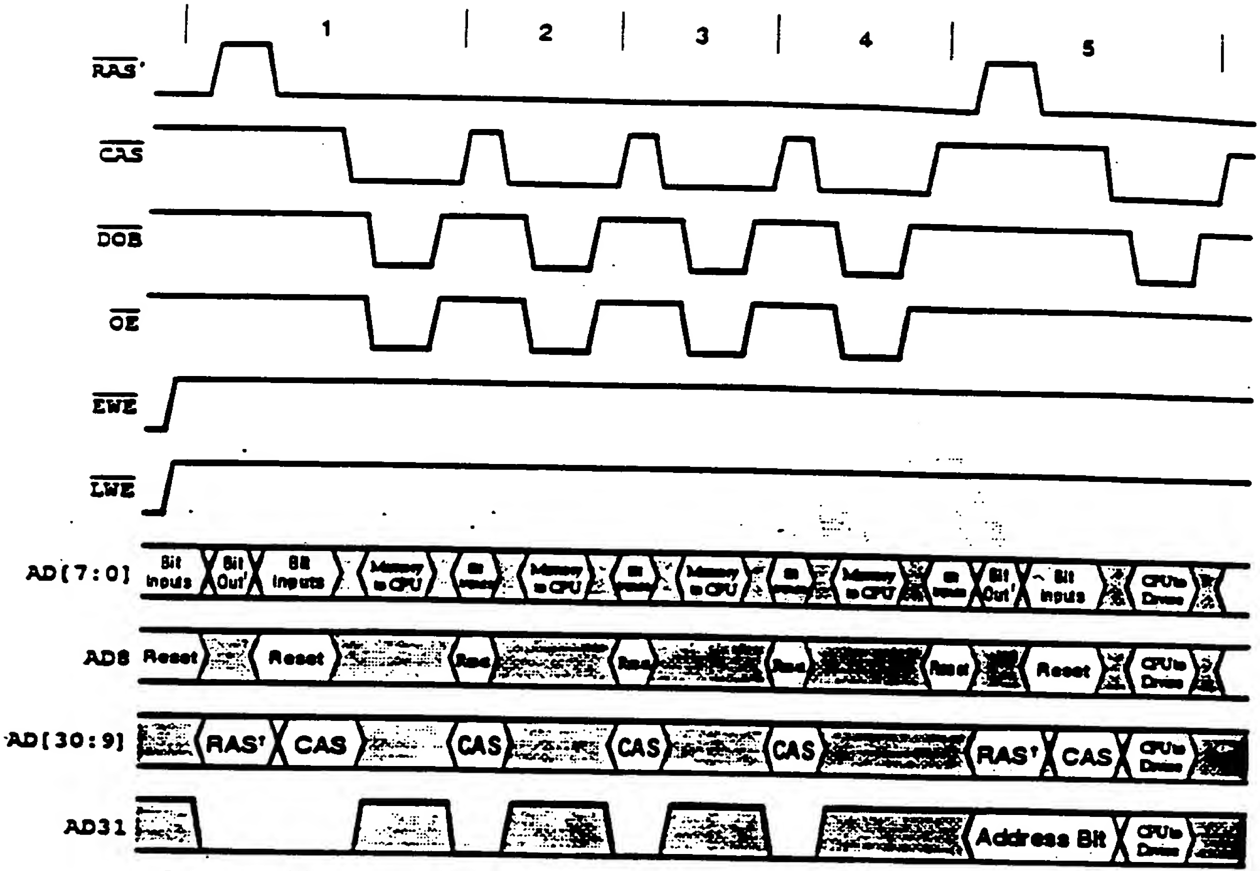

† Presence of RAS inactive period depends on system conditions.

FIG. 62

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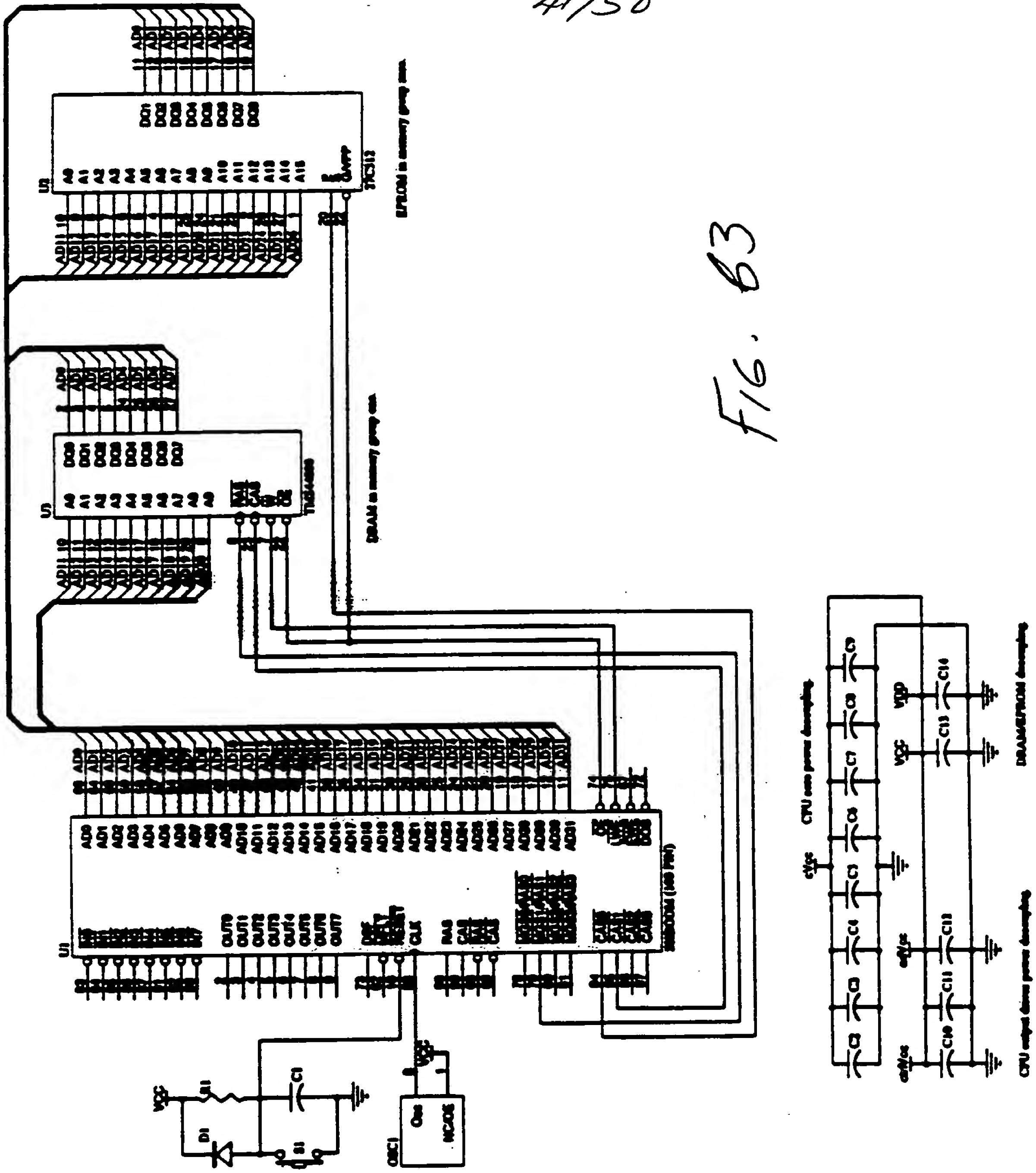

FIG. 63

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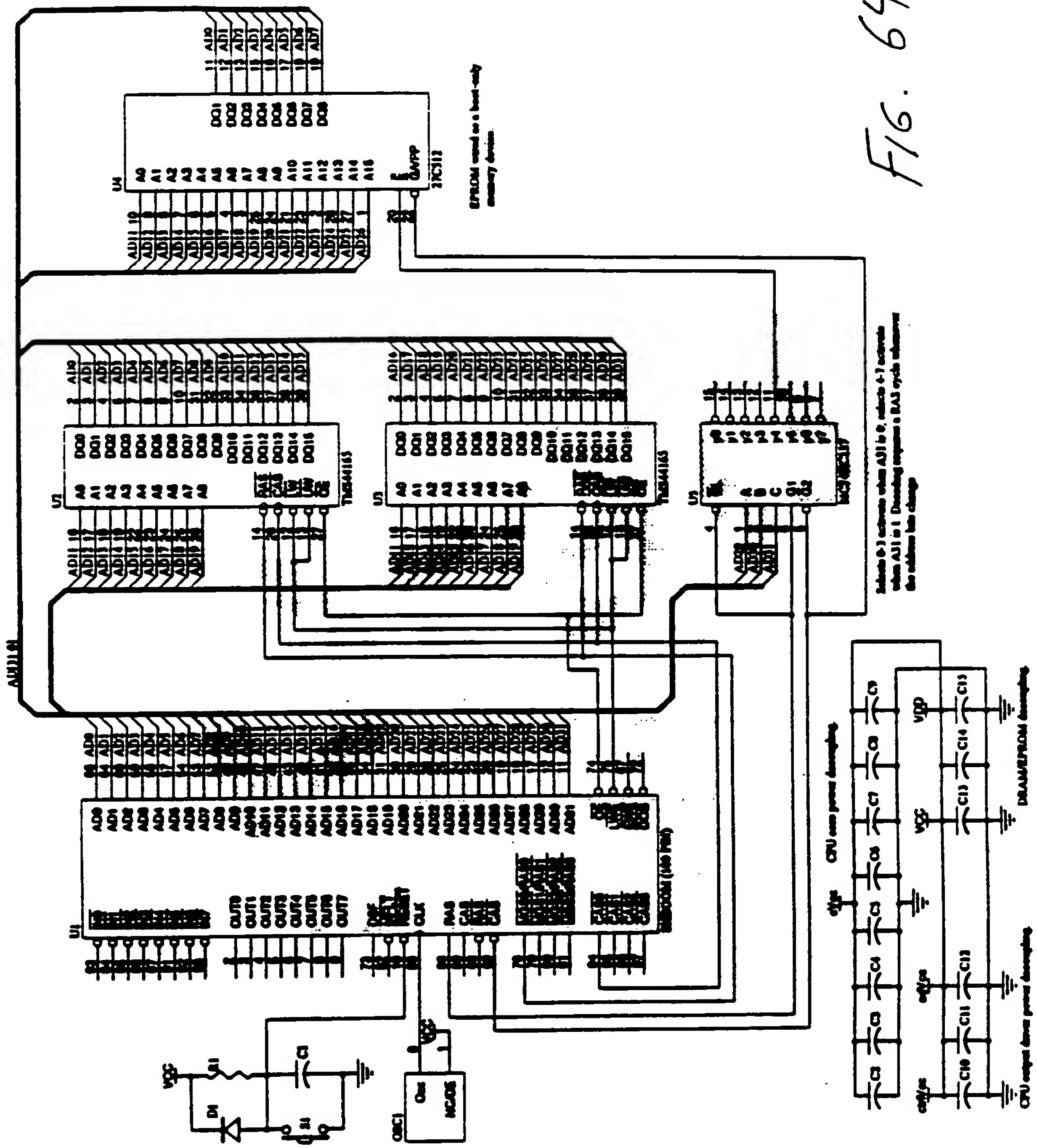

FIG. 64

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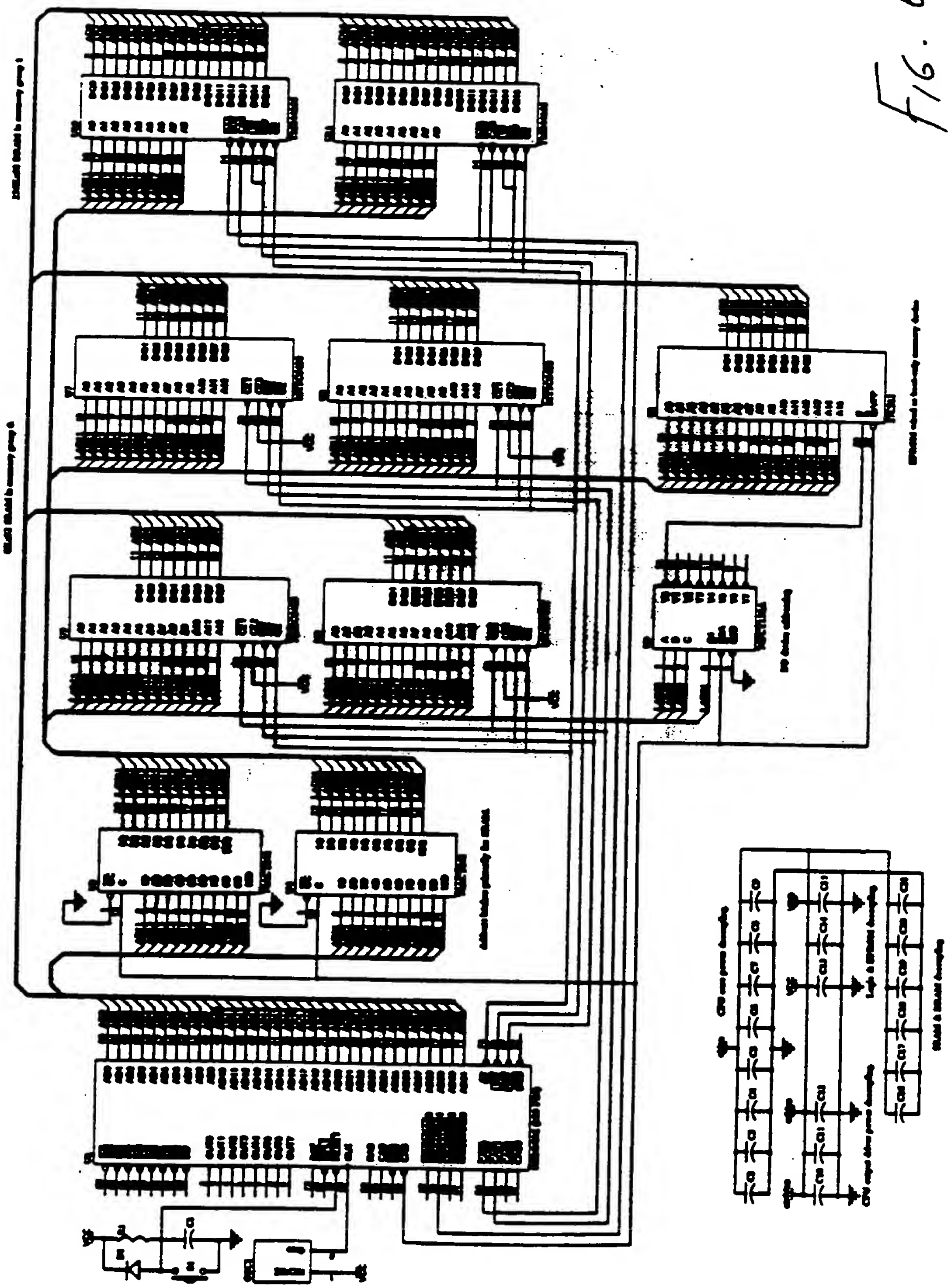

FIG. 65

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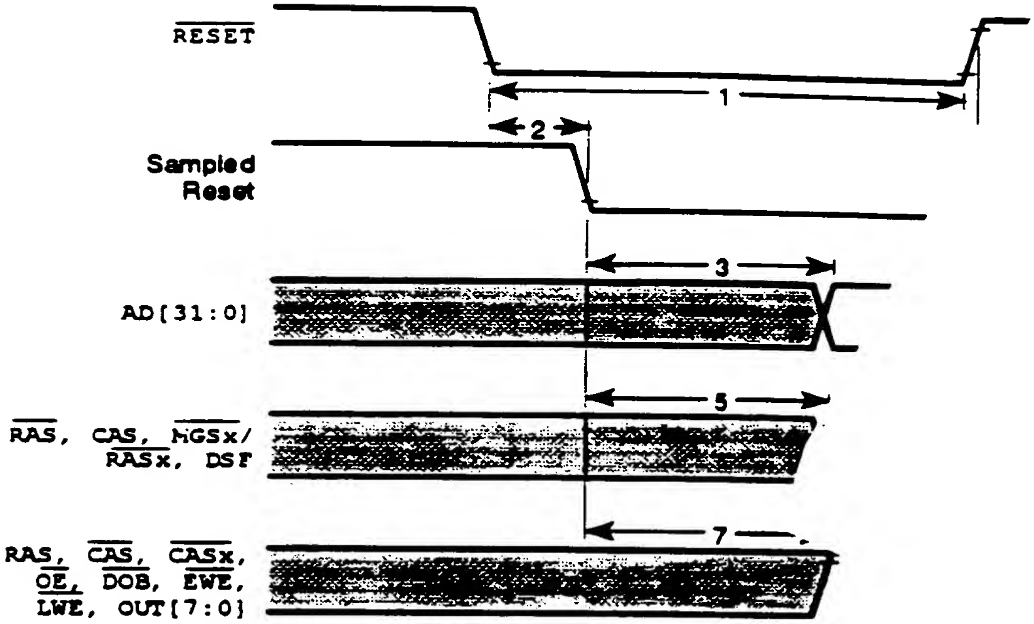

FIG. 66

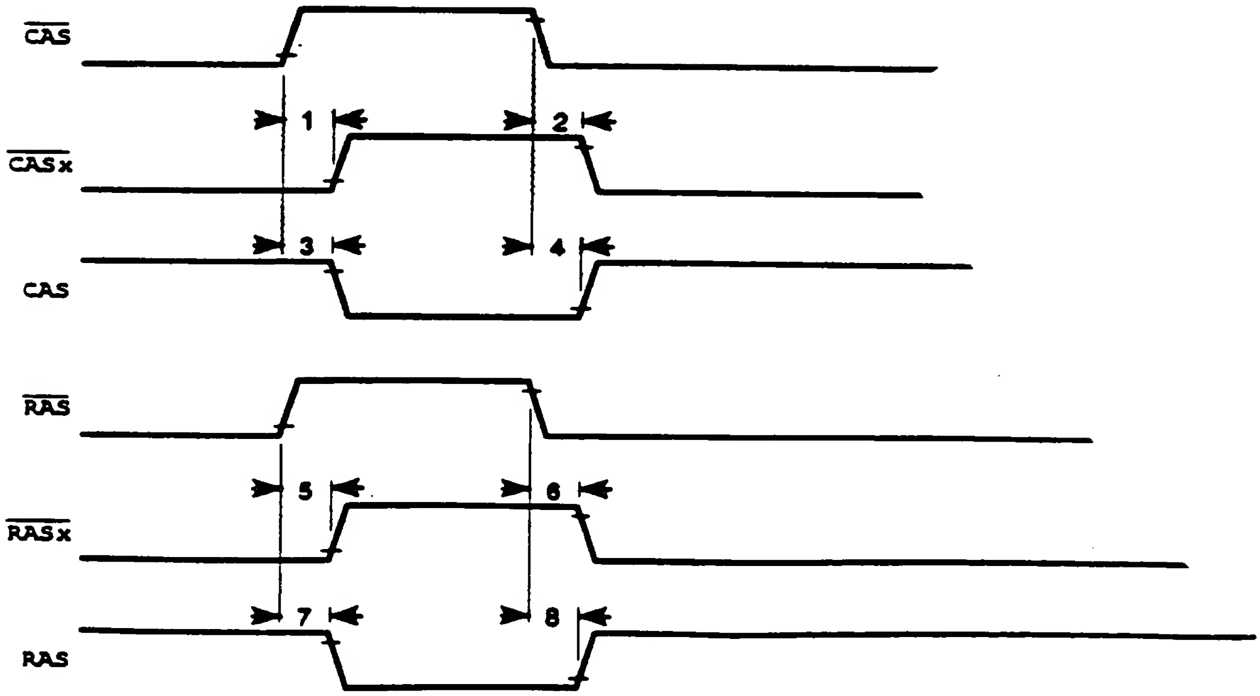

FIG. 69

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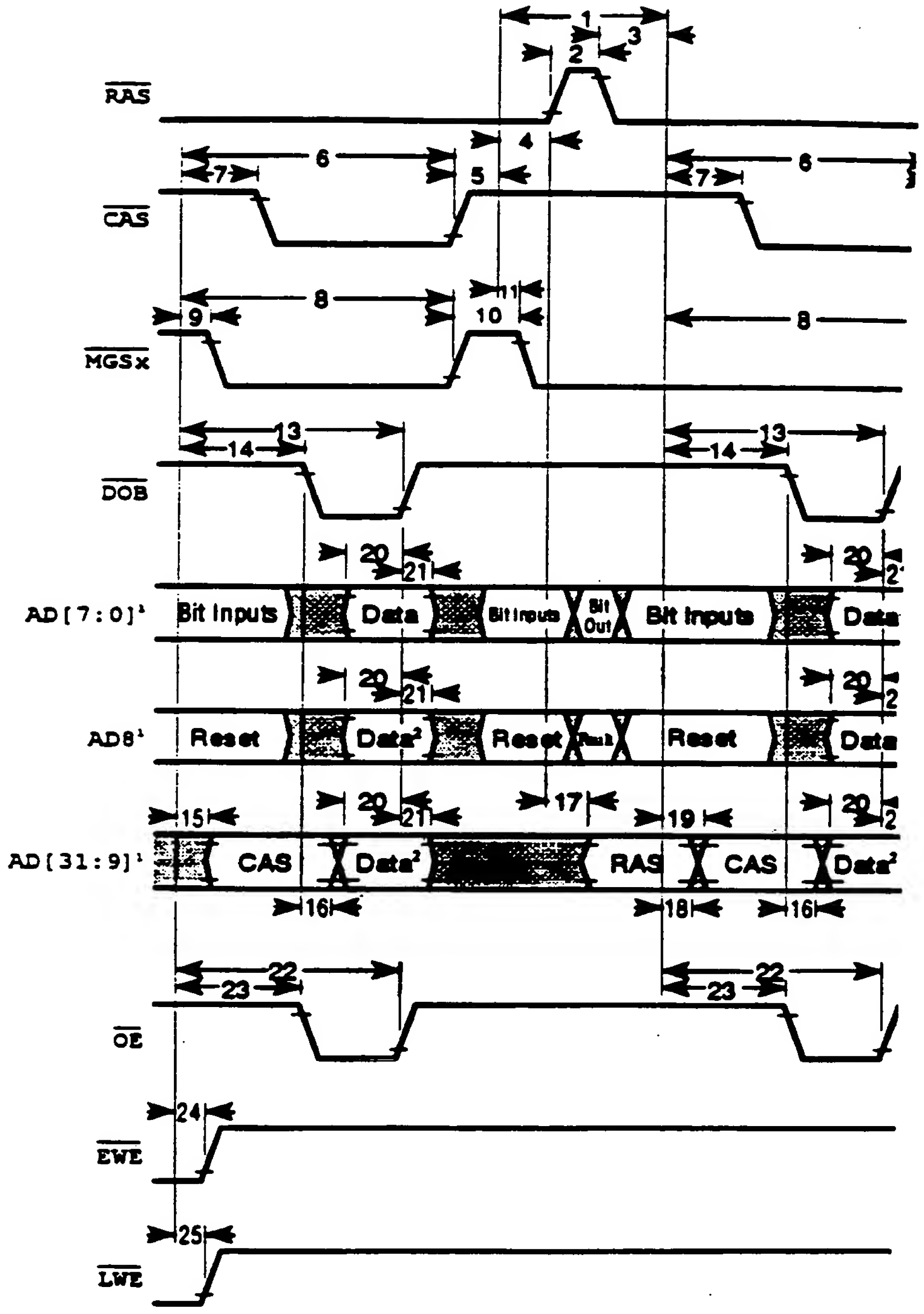
1
2
3
RAS
4
6
7
5
CAS
8
9
10
11
MGSx
13
14
DOB
20
21
AD[7:0]¹
Bit Inputs
Data
Bit Inputs
Bit Out
AD8¹
Reset
Data²
Reset
Reset
Data
15
17
19
AD[31:9]¹
CAS
Data²
RAS
CAS
Data²
16
18
22
23
OE
24
EWE
25
LWE

Fig. 67

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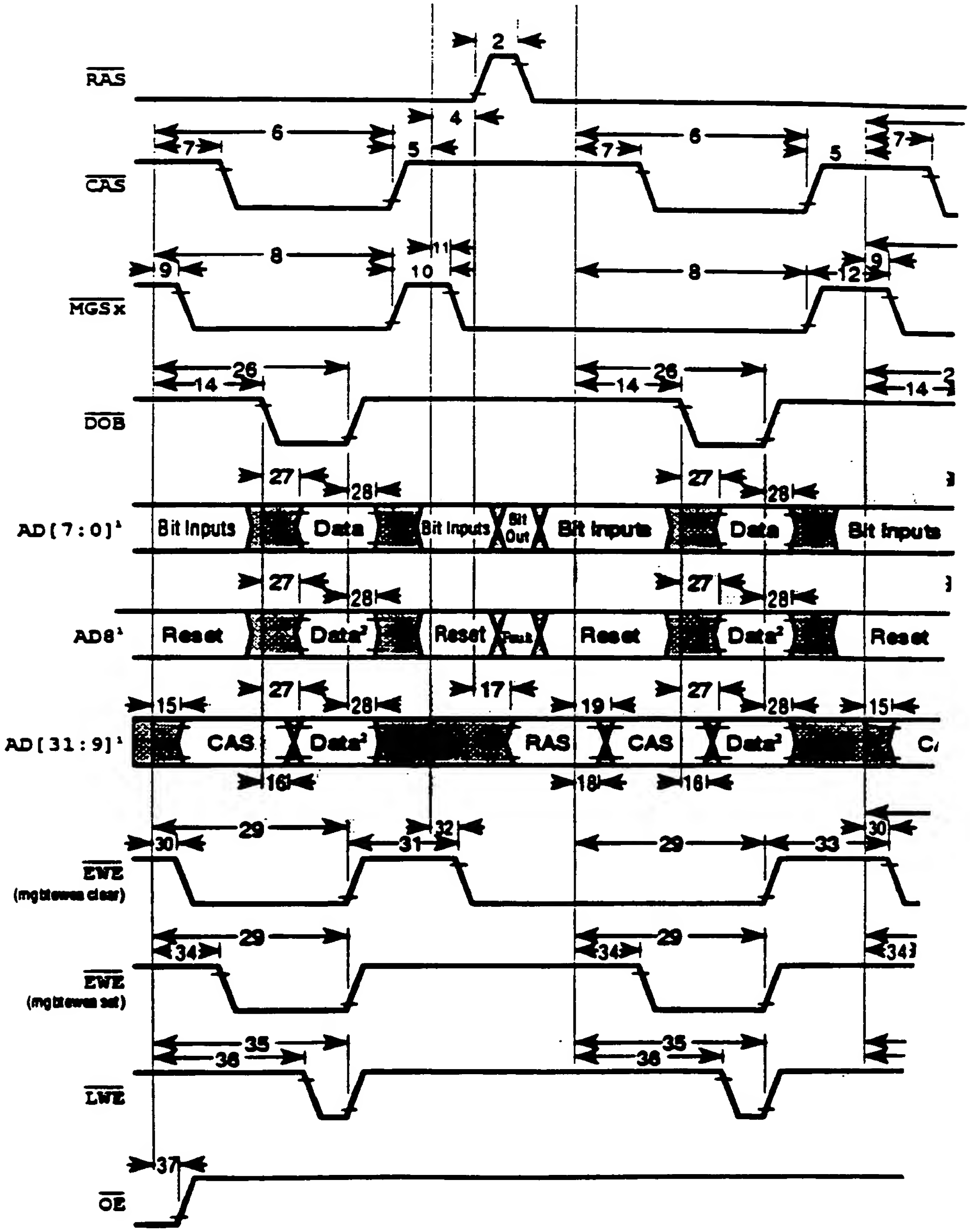

FIG. 68

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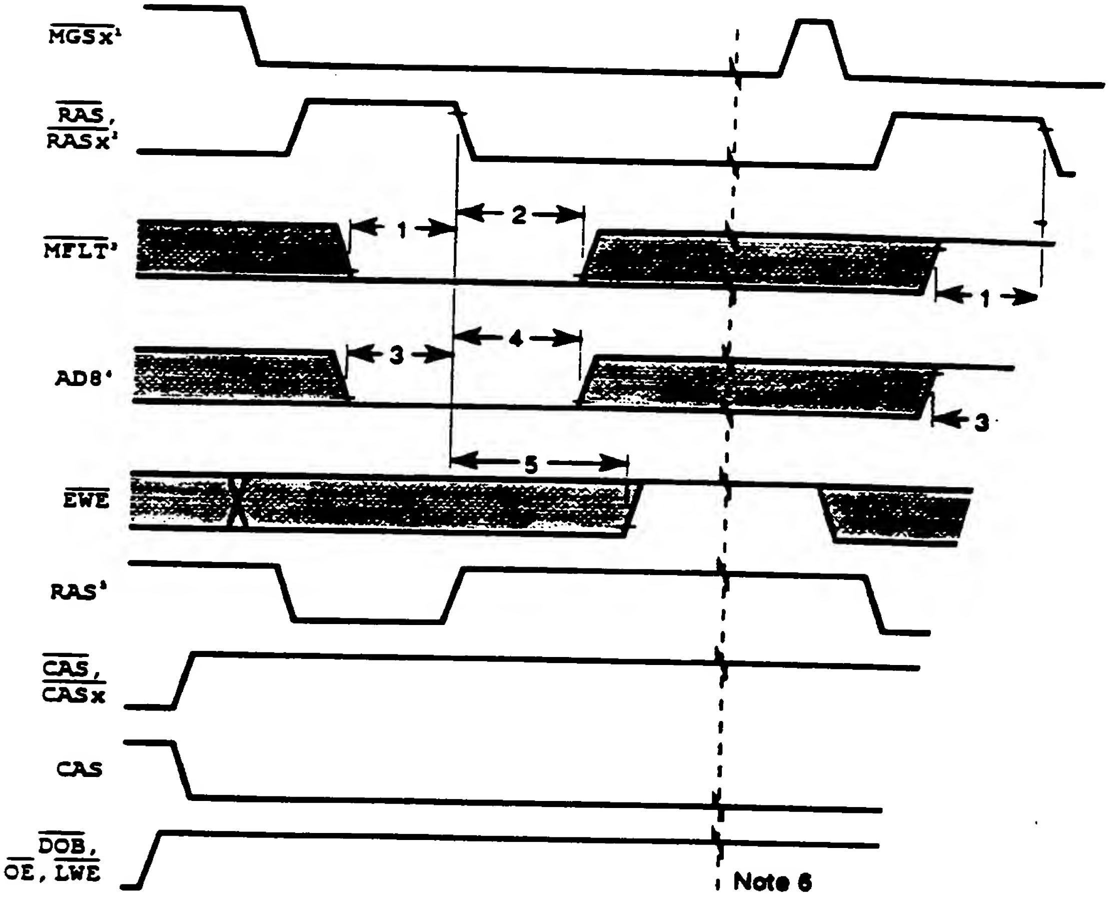

FIG. 70

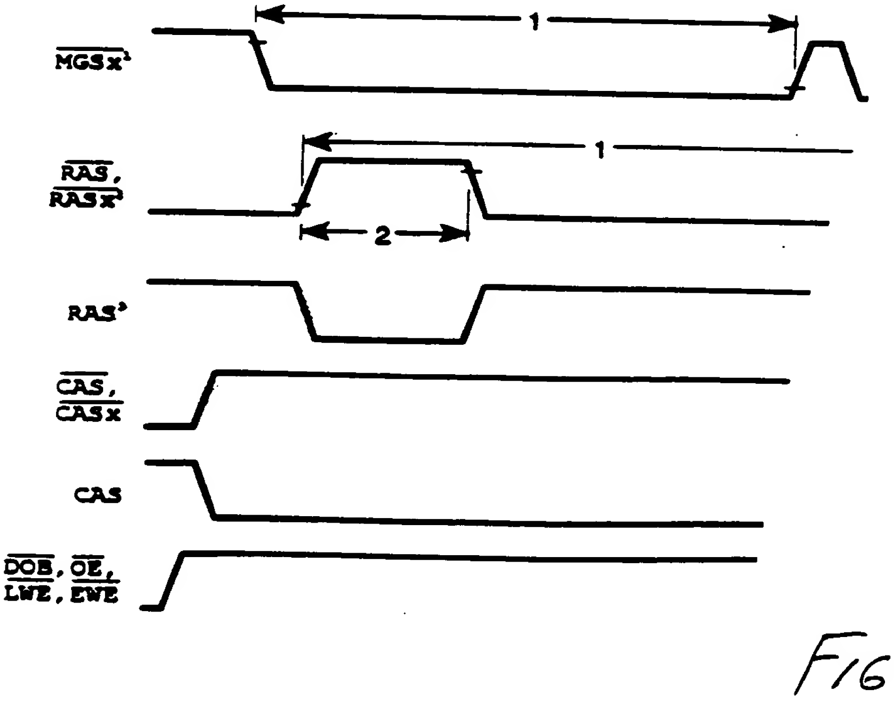

FIG. 71

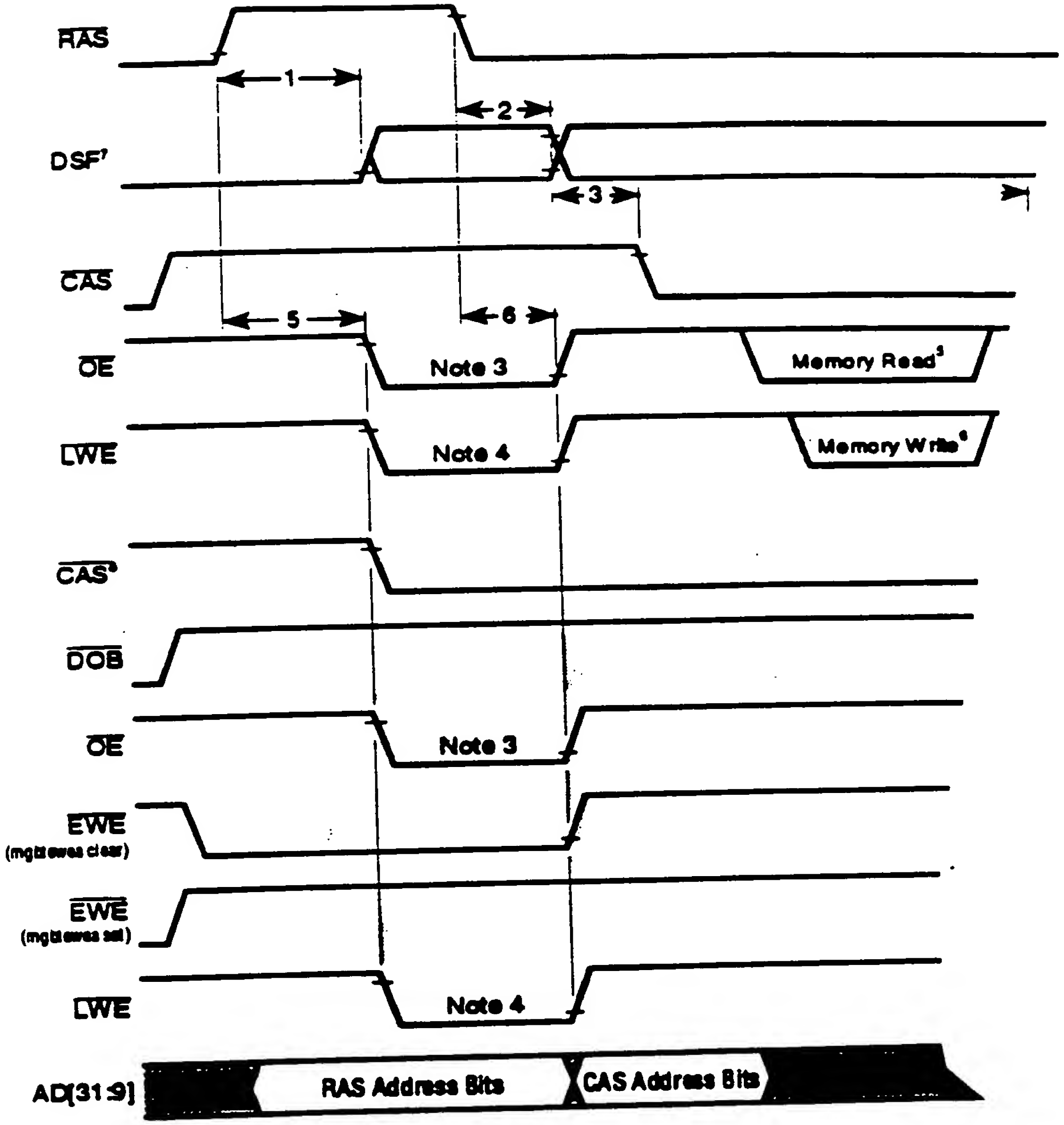
RAS
1
2
DSF7
3
CAS
5
6
OE
Note 3
Memory Read5
LWE
Note 4
Memory Write6
CAS8
DOB
OE
Note 3
EWE
(mgtlewes clear)
EWE
(mgtlewes set)
LWE
Note 4
AD[31:9]
RAS Address Bits
CAS Address Bits

FIG. 72

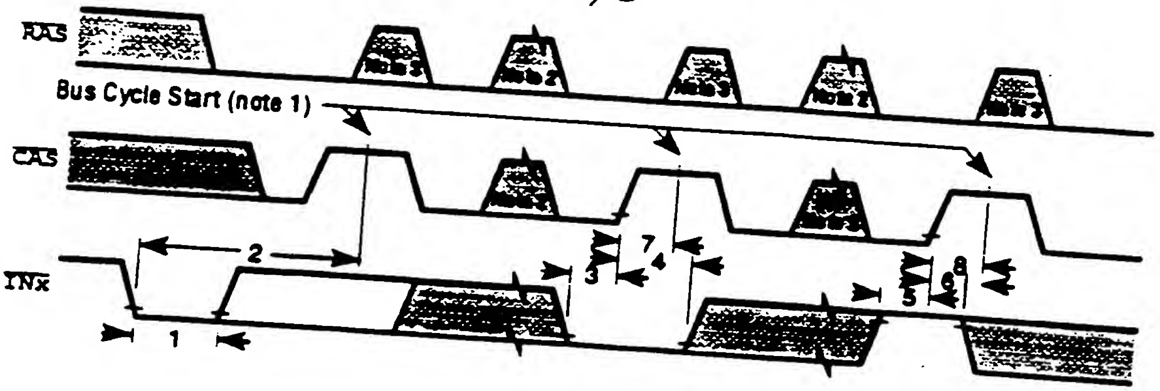

FIG. 73

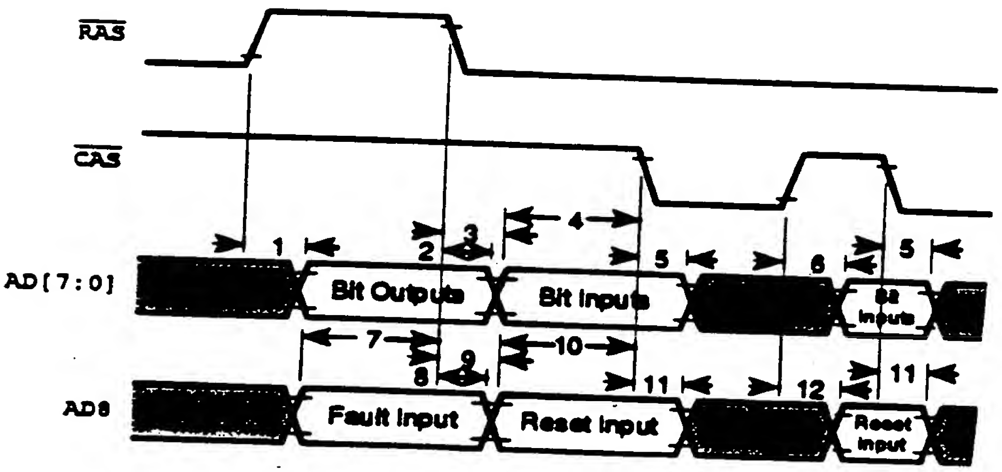

FIG. 74

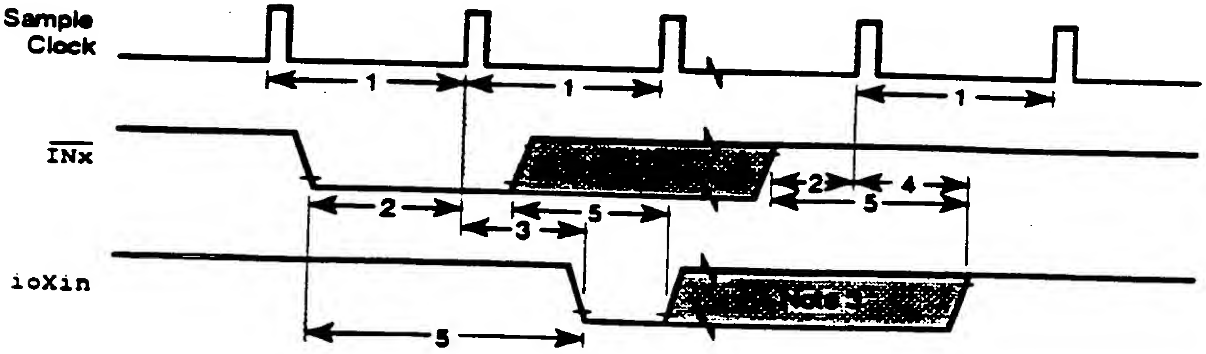

FIG. 75

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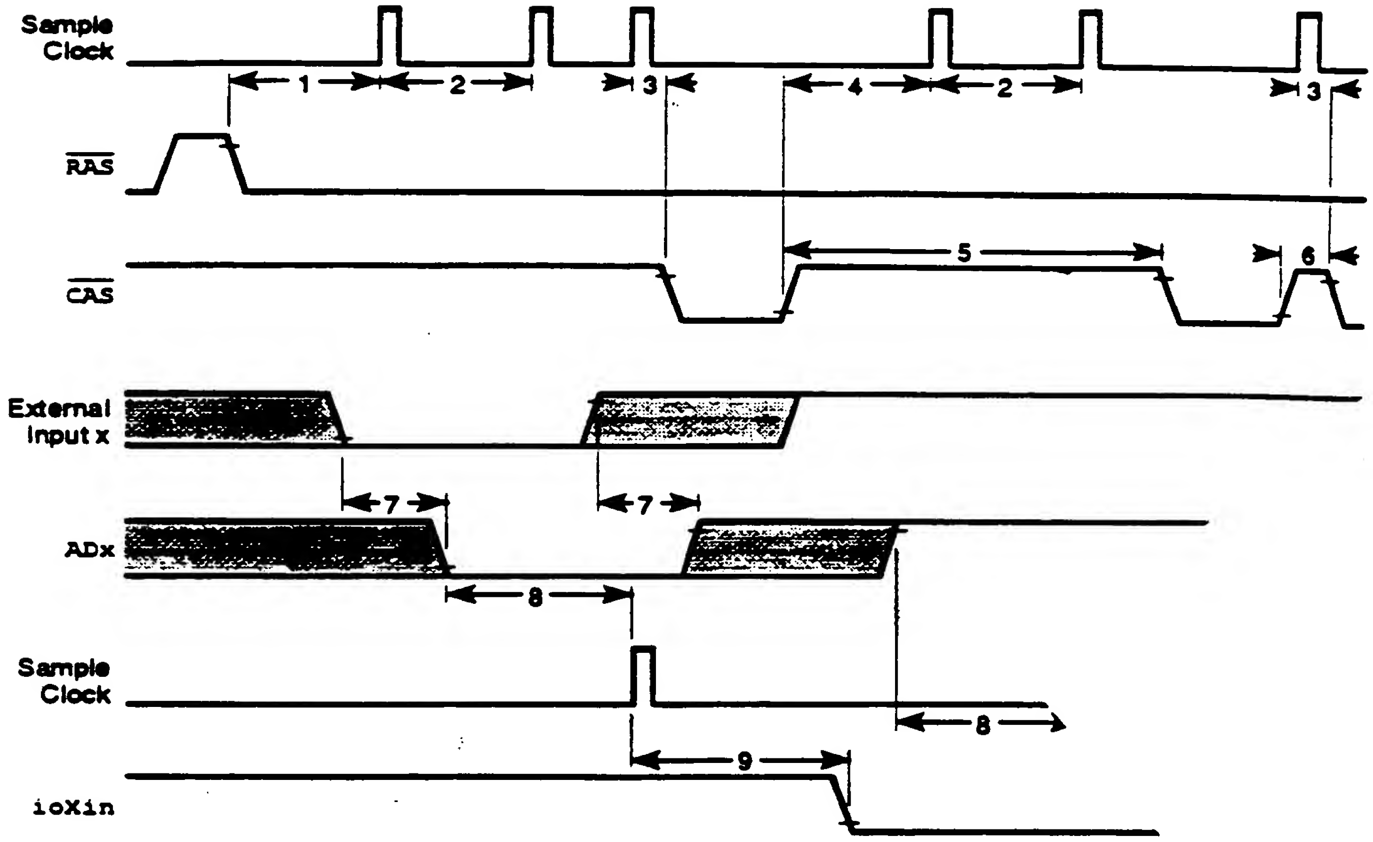
Sample Clock
RAS
CAS
External Input x
ADx
Sample Clock
ioXin
1
2
3
4
2
3
5
6
7
7
8
8
9

FIG. 76